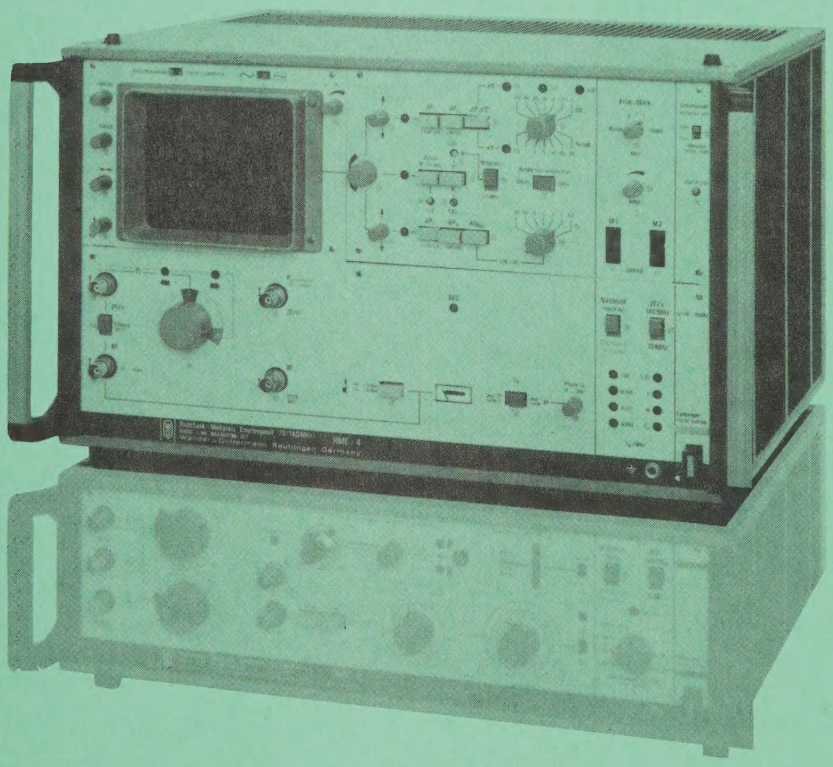
Service Manual



Receiving Section

(Wideband version)
for the radio-link measuring set-up RM-4

RME-4

BN 0697/00.83; Series H...

RECEIVING SECTION RME-4
(wideband version)

for the Radio-Link Measuring
Setup RM-4

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6. SERVICE MANUAL - PRELIMINARY REMARKS

6.1. Important Safety Advice

This instrument left the factory in a perfectly safe state. In order to maintain this state and to operate the instrument safely, we recommend that the following advice be carefully observed.

6.1.1. Opening The Instrument

When opening covers or removing parts with a tool, current-carrying parts may be exposed; connectors may also carry current.

Before the instrument is opened, it must be disconnected from all power sources.

If a calibration, maintenance or repair on an open, live instrument is unavoidable, this should be done only by a trained worker who knows the danger associated with the procedure.

Capacitors in the instrument may still be charged even though the instrument has been disconnected from all power sources; attention should be paid to circuit diagrams.

6.1.2. Fuses

Only the specified fuses may be used.

6.1.3. Repairs and Replacement of Parts

Repairs are to be carried out expertly. At the same time, special care is to be taken that the structural characteristics of the instrument are not altered so as to reduce safety. In

particular, the leakage path and the air path as well as the distances through the insulation must not be reduced.

Use only original parts as replacements. Other spare parts may be used only if they do not impair the safety properties of the instrument.

6.1.4. Tests After Repairs and Maintenance

Testing the Protective Conductor Connection

The proper connection and the condition is checked by inspection and by measuring the resistance between the protective conductor connection at the plug and the housing. The resistance should be < 0.5 Ω. The connecting lead should be moved during the measurement. Changes in resistance are an indication of damage.

Testing the Resistances of the Insulation

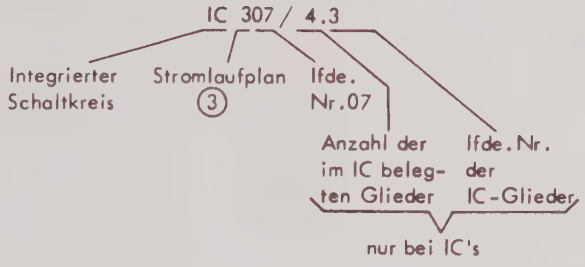
At 500 V, measure the resistance of the insulation between the power supply and the protective conductor connection. For this measurement, the mains switch of the instrument should be in the "on" position. The resistance of the insulation should be > 2MΩ.

6.2. Abbreviations, Symbols, etc.

6.2.1. Component Key

The individual components or circuit diagrams are numbered individually, e.g. (7). For this reason, the position numbers of all components, which are present in this group, commence with numeral 7.

The two subsequent numerals number the components consecutively, e.g. 06 in the capacitor C 706 or 11 in the resistance R 711. The prefixed letter describes the type of component (see Section 6.2.3.1.).



Key For Above Figure

Integrierter Schaltkreis	=	Integrated Circuit
Stromlaufplan	=	Wiring Diagram
lfde. Nr. 07	=	running No. 07
Anzahl der im IC belegten Glieder	=	Number of Sections occupied in the IC
lfde. Nr. der IC-Glieder	=	Running No. of the IC sections
nur bei IC's	=	only in the case of IC's

The individual connection (pin) of an IC component is identified by the pin No. behind the IC position number, e.g. IC 307-6.

When digital circuit symbols, e.g. delay sections with the notation DG (digital basic circuit) occur repeatedly within one circuit, they carry an additional lower-case letter - e.g. a - in the symbol of the wiring diagram. In the drawing of component parts, the same lower-case letter is a prefix of all concrete components of this digital circuit.

6.2.2. Components as Control Elements on Front Plate and Rear Wall of Instrument

Notwithstanding Section 6.2.1., components which at the same time are control elements of the instrument - switches, potentiometers, keys, jacks - are named in the service manual together with their abbreviation which is printed on the front plate and rear wall, e.g. [37] S 1402: switch for the intermediate frequency switch-over.

On the one hand, this enables the control element to be found quickly on the instrument when certain settings are prescribed, on the other, it is easier to find the control element in the circuit diagrams.

6.2.3. Abbreviations and Symbols

The abbreviations and symbols, given in Sections 6.2.3.1. and 6.2.3.2., are used for the different components in the service manual and in the circuit documentation.

6.2.3.1. Concrete Components

Bauelement	Abkürzung	Symbol
Batterie	B	
Buchse/Stecker	Bu/St	
Diode, Gleichrichter	Gl	
Z-Dioden	Gl	
Kapazitätsvariationsdiode	Gl	
Leuchtdiode	Gl	
Induktivität	L	
Anzeigeinstrument	J	
Kondensator, Trimmer	C	
Potentiometer	P	
Quarz	Q	
Relais	Rel	
Relaiskontakt	rel	
Schalter	S	
Sicherung	Si	
Signallampe	SL	
Transistor, bipolar	T	
Transistor Sperrschicht-Feldeffekt- (junction-FET)	T	
Transistor MOS-Feldeffekt- (metal oxid semiconductor-FET)	T	
Integrierte Schaltung	IC, JC	vgl. Abschnitt 6.2.3.2.
Übertrager	Ü	
Widerstand	R	
Heißleiter, Kaltleiter	R	

Key For Above Table:

Bauelement	=	Component
Abkürzung	=	Abbreviation
Batterie	=	Battery
Buchse/Stecker	=	Jack/Plug
Diode, Gleichrichter	=	Diode, Rectifier
Z-Dioden	=	Zener Diodes

Key For Above Table (Cont.):

Kapazitätsvariations-diode	=	Varactor
Leuchtdiode	=	Light-emitting Diode
Induktivität	=	Inductance
Anzeigeinstrument	=	Indicating Instrument
Kondensator, Trimmer	=	Trimmer Capacitor
Potentiometer	=	Potentiometer
Quarz	=	Quartz Crystal
Relais	=	Relay
Relaiskontakt	=	Relay Contact
Schalter	=	Switch
Sicherung	=	Fuse
Signallampe	=	Indicator Lamp
Transistor, bipolar	=	Transistor, bipolar
Transistor, Sperrschicht-Feldeffekt	=	Junction FET transistor
Transistor, MOS-Feldeffekt	=	Metal oxide semiconductor-FET transistor
Integrierte Schaltung	=	Integrated Circuit
vgl. Abschnitt	=	compare Section
Übertrager	=	Transducer
Widerstand	=	Resistance
Heissleiter, Kaltleiter	=	Thermistor/ptc resistor

6.2.3.2. Digital Symbols

Without claiming to be complete, the following is a list of some of the most important digital, graphical symbols. The two possible ranges of binary electrical quantity are described as L (low) and H (High). The value of the L range lies closer to $-\infty$ and the value of the H range lies closer to $+\infty$.

6.2.3.2.1. General Identification

Identification of the Negation

Of an Input:

Or an Output:

The dashed line indicates a portion of the border of a graphical symbol, for which the identification is used.

Identification of Dynamic Inputs

With the effect of an L/H edge

The effect is as if, on transition of the input signal from L to H, an H impulse is applied.

With the effect of an H/L edge

The same on transition from H to L.

Trigger Inputs (G Inputs)

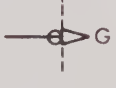
Static

with effect at H

with effect at L

single-edge controlled

with effect during L-H transition

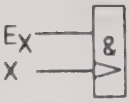
with effect during H-L transition 

two-edge controlled

with effect during L-H-L—impulse

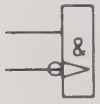
with effect during H-L-H-impulse

Identification of an Input Circuit With Preparation



E_X = prepared input
X = initiating input

The circuit supplies an H impulse on transition of the signal at X from L to H, if there previously is an H signal at the input E_X.

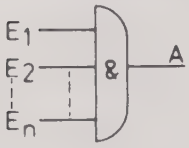


as above, however on transition from H to L.

Note: A possible retention time is to be stated!
(E_X)

6.2.3.2.2. Digital Linkage Section

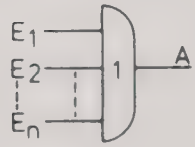
AND Section



E_1	E_2	A
L	L	L
L	H	L
H	L	L
H	H	H

An H signal appears at the output only when "H" is supplied to all inputs simultaneously (conjunctive linkage).

OR Section



E_1	E_2	A
L	L	L
L	H	H
H	L	H
H	H	H

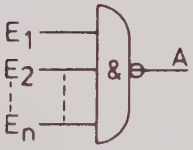
An H signal appears at the output when "H" is supplied to at least one input (disjunctive linkage).

NOT Section

E	A
H	L
L	H

The reverse of the input signal always appears at the output (inverting).

NAND Section

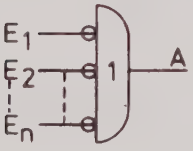


E_1	E_2	A
L	L	H
L	H	H
H	L	H
H	H	L

An L signal appears at the output when "H" is supplied to all inputs.

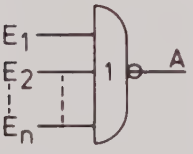
A Different Type of Representation:

This is obtained from the DE MORGAN Theorem from the relationship:



$$A = \overline{E_1 \wedge E_2 \wedge \ldots E_n}$$
$$A = \overline{E_1} \vee \overline{E_2} \vee \ldots + \overline{E_n}$$

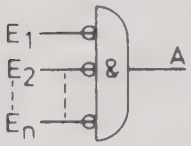
NOR Section



E_1	E_2	A
L	L	H
L	H	L
H	L	L
H	H	L

An L signal appears at the output when "H" is supplied to at least one input.

According to the DE MORGAN redrawn representation:



$$A = \overline{E_1 \vee E_2 \vee \ldots + E_n}$$
$$A = \overline{E_1} \wedge \overline{E_2} \wedge \ldots \overline{E_n}$$

Differentiating Section

Circuit which converts an L/H edge into an L-H-L spike impulse.

Circuit which converts an H/L edge into an H-L-H spike impulse.

AND Linkage by Wiring ("Wired AND")

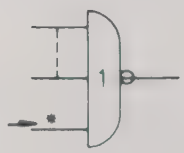
A circuit which, by leaking the outputs of two or more elements, puts into effect an AND linkage without using an actual AND section.

NOR Gate With a So-Called "Power" Output

The thickening of the border on the output side characterizes the higher load-carrying capacity (in the case of IC's this is described as higher "fan out").

Enlargement of the Input Circuit through a so-called "expander" input.

Example:



NOR steps with four inputs. An additional special input permits the enlargement of the linkage through external wiring.

6.2.3.2.3. Sweep Circuits With Storage Behavior

We differentiate between two basic types, the flip-flop (FF) and the monoflop (MF).

Flip-flops

This sweep circuit has two stable positions. The flip-flop occupies one or both positions, depending on the input signal.

If one of the two positions is fixed as the normal position, then that output, which assumes the H condition is characterized by a black beam.

Static Input Signals (Explanation and Examples)

If the signal at the input E_1 changes from L to H, the FF flips independently of the slope of the L-H transition into the position, which is characterized by an H condition at the output A_1. The output A_2 is then necessarily in the L state.

If the signal at the input E_1 changes from H to L, the FF remains in the previously assumed position. Only when the signal at input E_2 changes from L to H, does the FF flip into the second stable position, which is characterized by an H state at the output A_2. (Here assumed to be the normal position).

An L state necessarily exists then at output A_1. The FF retains this position even when the signal at the input E_2 changes from H to L.

In general, it is not permissible to supply a signal with L-H transitions simultaneously to the inputs E_1 and E_2.

E_1	E_2	A_1	A_2
H ↓	L	H	L
L ↓	L ↓	H ↓	L ↓
L	H ↓	L ↓	H ↓
L ↓	L	L ↓	H
H ↓	L	H ↓	L ↓
H	H ↓		

← no FF behavior

If a flip-flop field has several inputs without special identification, then these inputs are linked disjunctively (OR linkage).

This means:

The flip-flop flips as a signal changes from L to H at input E_1 or input E_2 or at both inputs into the position which is characterized by an H state at the output A_1.

In the following example, the inputs E_1 and E_2 are linked conjunctively (AND linkage).

This means:

The flip-flop flips only when both inputs E_1 and E_2 simultaneously assume the H state.

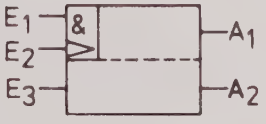
Examples With Dynamic Input Signals

The flip-flop below has two dynamic inputs E_1 and E_2. A L/H edge at E_1 flips the flip-flop into the position which is characterized by an H state at the output A_1. In the same manner, an L/H edge at E_2 flips the flip-flop into the position, which is characterized by an H state at the output A_2.

If the symbol ▷ (or ⧐) is at the line dividing the two fields, the flip-flop flips at each L/H (or H/L) edge, A_1 and A_2 being alternately characterized by H (or L).

Flip-Flop With Preparation

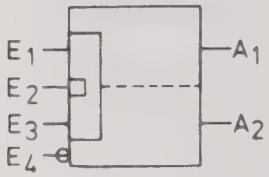
An L/H edge at the dynamic input E_2 is operational only when the preparation input E_1 simultaneously is in the H state. In this case, the flip-flop flips into the position which is characterized by an H state at the output A_1. E_3 is a static input.



In the following graphical symbol, the dynamic input with preparation acts on both fields, that is, each L/H edge at input E_2 flips the flip-flop when an H state exists simultaneously at input E_1.

Flip-Flops From Integrated Circuits

J-K Master-Slave Flip-Flop (e.g. SN 7473 from Texas)



t_n		$t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

t_n = Time before synchronizing impulse

t_{n+1} = Time after the synchronizing impulse

E_2 = Timing input

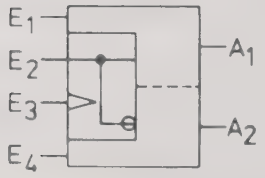
E_4 = Asynchronous reset input (independent of E_2) L Potential at E_4 brings Q to an L signal

$J = E_1$

$K = E_3$

$Q = A_1 = \overline{A}_2$

D-Type Flip-Flop (edge-triggered) (also as example of SN 7474 from TI)



t_n		$t_n + 1$
E_2	A_1	A_2
L	L	H
H	H	L

FF with prepared input E_2 and an overriding, initiating input E_3. E_1 and E_4 act directly on the outputs.

Monoflops

This type of flip-flop circuit is characterized by the fact that it can assume only one stable position (rest position) and a quasi-stable position (operating position), the arrow indicating the field whose output is in the resting position.

Example:

In the following monoflop, an H state at the static input E_1 or an L/H edge at the dynamic input E_2 flips the circuit from the rest position into the quasi-stable operating position (H state at output A_1).

After the flyback time t_R, whose duration is determined by an internal RC section, the monoflop flips back into the rest position.

6.2.3.2.4. Delay Sections

delays the transition from L to H

delays the transition from H to L

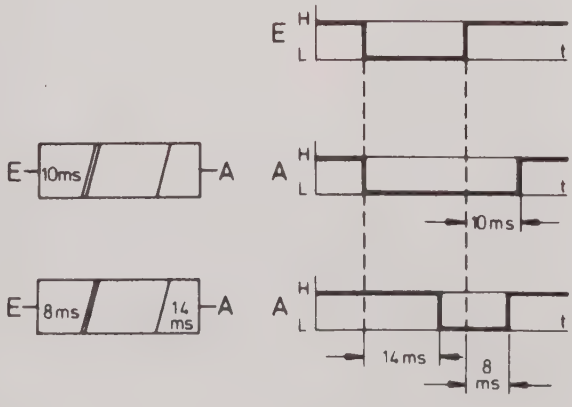
delays the transition from H to L as well as from L to H, however by unequal times.

delays the transitions from L to H and from H to L by equal times.

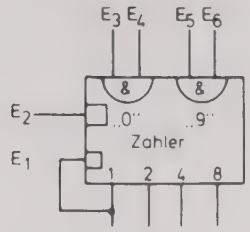
The double inclined lines identify the input side.

The delay time can be entered in time units, e.g. in ms or µs.

Examples of the Application



6.2.3.2.5. BCD Counting Decade as Integrated Circuit



Zähler = Counter

Conditions for Setting to Numeral 0:

E_3 and E_4 to H state,

E_5 or E_6 or both in L state.

Conditions for Setting to Numeral 9:

E_5 and E_6 to H state,

E_3 or E_4 or both in L state.

At each of the two AND sections, at least one input must be in the low state during counting (impulse input E_2).

Ziffer	Ausgänge			
	1	2	4	8
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Key For Above Table:

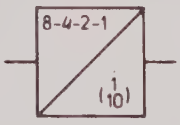
Ziffer = Numeral

Ausgänge = Outputs

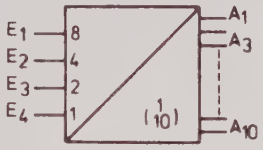
6.2.3.2.6. Code Converter as Integrated Circuit

Simplified Representation

(Example)



Representation with the individual inputs and outputs

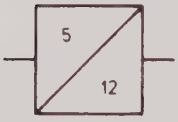


Converting the BCD Code 8-4-2-1 into the 1-out-10 Code

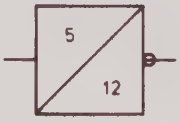
6.2.3.2.7. Switching Stages

The representation of switching stages of any kind (input, output, transistor stages which have the function of a level converter.

with an input



a) not inverting



b) inverting

6.2.4. Further Additional Abbreviations

(2) = sub-assembly (2) = circuit (2)

[697-L] = printed circuit board L

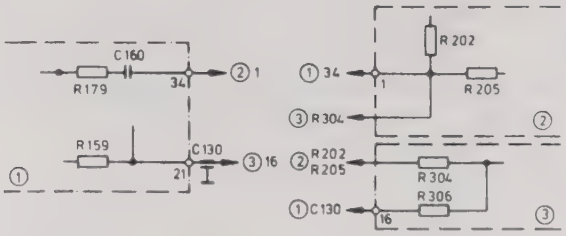
Pkt. 6 = connection point 6

TP 303 = test point 303
(in sub-assembly (3))

6.2.5. Sub-Assembly Connections

Since the circuit diagrams in the appendix are drawn separately for each sub-assembly, all wires leading to a different

sub-assembly, must be clearly recognizable. The sketch below explains the procedure used here for their identification.



In the sketch, point 34 of component (1) is connected to point 1 of component (2), C 130 of component (1) is connected to point 16 of component (3) and R 304 of component (3) is connected to the common connection point of R 202 and R 205 of component (2).

6.3. Advice For Ordering Spare Parts

The most important information concerning spare parts required may be taken from the table of replaceable parts. Components with Bv. or WN numbers are to be ordered from the plant. When ordering spare parts, it is important to state the order number (BN), as well as the instrument number and the position number of the component, e.g.

BN 697/Nr. 525070 B/T 202

The white type shield, with order number and instrument number, is on the left side of the rear wall. The necessary particulars for ordering replacement printed circuit boards can be taken from the circuit diagrams. These particulars consist of a framed number-letter combination, e.g. 697-H. The complete particulars for ordering would look as follows:

BN 697/Nr. 525070 B/697-H

6.4. Necessary Instruments

The instruments required for service work are listed in the following table. They represent recommendations. Equivalent instruments of other manufacturers may also be used.

Service work on the plug-in cards of the upper right plug-in card is facilitated by the use of the adaptor cards 697-AT and 697-BK. The adaptor cards permit the plug-in cards to be operated outside of the basic instrument.
They can be supplied as measuring accessories via W & G.

Gerät	Verwendeter Typ		in Abschnitt
Digitalmultimeter (3 1/2 stellig)	8000 A	Fluke	7.3.1./7.3.2./7.3.3./7.3.5./7.3.14./9.1./9.20.3.
Digitalmultimeter (4 1/2 stellig)	8600 A	Fluke	9.5./9.8./9.14./9.15./9.16./9.17./9.20.4.
Frequenzzähler (bis 25 MHz)	FZ-4	W&G	7.3.9./9.15./9.19.
Frequenzzähler (bis 150 MHz)	5382 A	hp	7.3.7./9.12.
RF-Millivoltmeter mit VHF-Tastkopf	411 A 11023 A	hp	7.3.3./7.3.5./7.3.6./7.3.7./7.3.8./7.3.12./7.3.13./9.10./9.18.
Oszilloskop mit 10 : 1-Tastkopf	PM 3240 PM 9350	Philips	7.3.2./7.3.4./7.3.5./7.3.6./7.3.7./7.3.10./7.3.11./7.3.12./7.3.13./7.3.14./9.14./9.16./9.17./9.19.
Pegelsender	PS-14 (Hinweis: PS-14 ist Teil des PSM-14)	W&G	7.14.
Selektiver Pegelmesser mit Tastkopf	SPM-14 TK-11 (Hinweis: SPM-14 ist Teil des PSM-14)	W&G	7.3.9./9.17.
Selektiver Pegelmeßplatz	PSM-14	W&G	8.1.1./8.4.2./8,9.1./9.7.
Reflexionsmeßbrücke zum PSM-14	RFZ-5	W&G	8.4.2.
Richtfunk-Meßplatz	RM-4	W&G	8.4.1./9.6.
Reflexionsmeßbrücke zum RM-4	RFZ-4	W&G	8.4.1./9.6./9.16.
Eichpegelmesser mit Tastkopf	EPM-1 TK-10	W&G	8.5./9.3./9.16.
NF-Meßgerät	PMG-2	W&G	8.9.2.
Funktionsgenerator	Model 180	Wavetek	9.17.
Klirranalysator	SPM-11/PSE-11	W&G	9.19.
Rauschklirrmeßplatz	RK-50	W&G	8.8.
Bandbegrenzungsfilter für 1800-Kanal-System	RSB-316/8160	W&G	8.8.
für 2700-Kanal-System	RSB-316/12360	W&G	8.8.

Gerat	Verwendeter Typ		in Abschnitt
Bandsperren für die Meßfrequenzen 534, 1248, 2438, 5340, 7600 und 11700 kHz	RSS-534, ..., RSS-5340, W&G ..., RSS-11700		8.8.
Umsetzereinschübe für die vorstehenden Meßfrequenzen	REU-534, ..., REU-5340, W&G ..., REU-11700		8.8.
Preemphase-Netzwerk für 1800-Kanal-System für 2700-Kanal-System	 BN 445/12 BN 445/13	 W&G	8.8.
Deemphase-Netzwerk für 1800-Kanal-System für 2700-Kanal-System	 BN 446/12 BN 446/13	 W&G	8.8. 9.8.
Gleichspannungsstabilisator	GS-2	W&G	9.9.
X-Y-Schreiber	7035 B	hp	8.1.1./9.7.
2-Wege-Verteiler	REV-56	W&G	8.8.
5-dB-Dämpfungsglied, Z = 75 Ω			8.9.1./8.9.2.
6-dB-Dämpfungsglied, Z = 75 Ω			9.5.
20-dB-Dämpfungsglied, Z = 75 Ω			8.9.2.
Abschlußwiderstand 75 Ω			8.9.2.
Reihenwiderstand 75 Ω			8.4.1./9.6.
T-Stück, Z = 75 Ω			7.3.14./9.20.4.
Hochspannungstastkopf	80 K-40	Fluke	8.8.
Fernsteuerkabel	K 176	W&G	

Key For Above Table:

Gerät	=	Instrument
Verwendeter Typ	=	Type used
in Abschnitt	=	in Section
Digitalmultimeter	=	Digital multimeter
stellig	=	positions
Frequenzzähler	=	Frequency counter
bis	=	to
RF-Millivoltmeter mit VHF-Tastkopf	=	RF millivoltmeter with VHF sensing head
Oszilloskop mit 10:1-Tastkopf	=	Oscilloscope with 10:1 sensing head
Pegelsender	=	Level transmitter
Hinweis: PS-14 ist Teil des PSM-14	=	Hint: PS-14 is part of PSM-14
Selektiver Pegelmesser mit Tastkopf	=	Selective level meter with sensing head
Hinweis: SPM-14 ist Teil des PSM-14	=	Hint: SPM-14 is part of PSM-14
Selektiver Pegelmessplatz	=	Selective level measuring set up

Key For Above Table (Cont.):

Reflexionsmessbrücke zum PSM-14	=	Return loss measurement bridge for PSM-14
Richtfunk-Messplatz	=	Directive radio beacon measuring set up
Reflexionsmessbrücke zum RM-4	=	Return loss measurement bridge for RM-4
Eichpegelmesser mit Tastkopf	=	Calibrated level measuring instrument with sensing head
NF-Messgerät	=	VLF measuring instrument
Funktionsgenerator	=	Waveform generator
Klirranalysator	=	Distortion analyzer
Rauschklirrmessplatz	=	White noise measuring set up
Bandbegrenzungsfilter	=	Band-limiting filter
für 1800 Kanal System	=	For 1800 channel system
für 2700 Kanal System	=	For 2700 channel system
Bandsperren für die Messfrequenzen	=	Band-stop filters for the measuring frequencies
und	=	and
Umsetzereinschübe für die vorstehenden Messfrequenzen	=	Convertor plug-in units for the above measuring frequencies
Preemphase-Netzwerk	=	Pre-emphasis network
Deemphase-Netzwerk	=	De-emphasis network
Gleichspannungsstabilisator	=	DC stabilizer
X-Y—Schreiber	=	X-Y-Recorder
2-Wege-Verteiler	=	2-way distributor
5-dB Dämpfungsglied	=	5 dB damping section
Abschlusswiderstand	=	Terminating resistance
Reihenwiderstand	=	Series resistance
T-Stück	=	T- piece
Hochspannungstastkopf	=	high-voltage sensing head
Fernsteuerkabel	=	Remote-control cable
T-Verzweigung	=	"T" brancher
Eichleitung	=	Calibrated attenuator
Digitaler Taster	=	Digital sampler
Sichtgerät	=	Display Unit
Horizontalverstärker	=	Horizontal amplifier
Vertikalverstärker	=	Vertical amplifier

7. ADVICE FOR TROUBLE SHOOTING AND FOR MAKING REPAIRS

The following sections contain information required for trouble shooting and for sectionalizing the trouble. When trouble shooting, the emphasis should be on functional defects and not on tolerance defects, the latter being defined as defects which exceed a maximum error without impairing the function of the instrument to any noteworthy extent.

Trouble shooting is carried out with the help of trouble-shooting plans.

A further aid in trouble shooting is the appendix for operating and servicing instructions with block and individual circuit diagrams, drawings of component parts and tables of replaceable parts. Chapter 10, DESCRIPTION OF THE FUNCTIONS, is intended to be of help in understanding the circuit diagrams.

In order to make trouble shooting easier, all important views of the instrument have been reproduced in the following and the position of the sub-assemblies and the measuring points have been reproduced.

For repair work, the dismantling descriptions in Section 7.4 are to be taken into consideration.

Advice: We recommend that the user of the radio-link measuring setup RM-4 does not repair any defects discovered in the wideband demodulator (27), because considerable testing and measuring equipment is required for the subsequent alignment. Instead, the user may turn to the nearest W & G Service Office or directly to the

Customer Service Division VIS at the Eningen plant. A replacement demodulator is held in readiness in the Customer Service Division for exchange purposes. The disassembly of the demodulator component is described in Section 7.4.5.

7.1. Preparation of the Instrument for Trouble Shooting

Lid, bottom and left side wall are to be removed for trouble shooting. For this purpose, the instrument is advisably placed on the right side wall (with power supply).

The hexagonal pin spanner supplied (SW3), which is attached to a holder at the rear wall of the instrument, is to be used for loosening the hexagonal socket-head bolts, which connect the lid and bottom with the side walls.

After those sections of the housing, which have been loosened, have been taken off, the instrument plug-in units with the circuit plates are exposed. The visual part and the upper right plug-in part, which are mechanically connected with one another, may be separated from the lower plug-in part by a sideways displacement in the guide grooves of the right rear wall.

It is moreover also possible to separate the visual part from the upper right plug-in part by loosening the mechanical connecti with the assembly spanner supplied (see Figure 7-1).

The length of the electrical connections between the individual plug-in parts is such that they do not have to be undone when the instrument is disassembled. The instrument remains fully

functional even in the disassembled state!

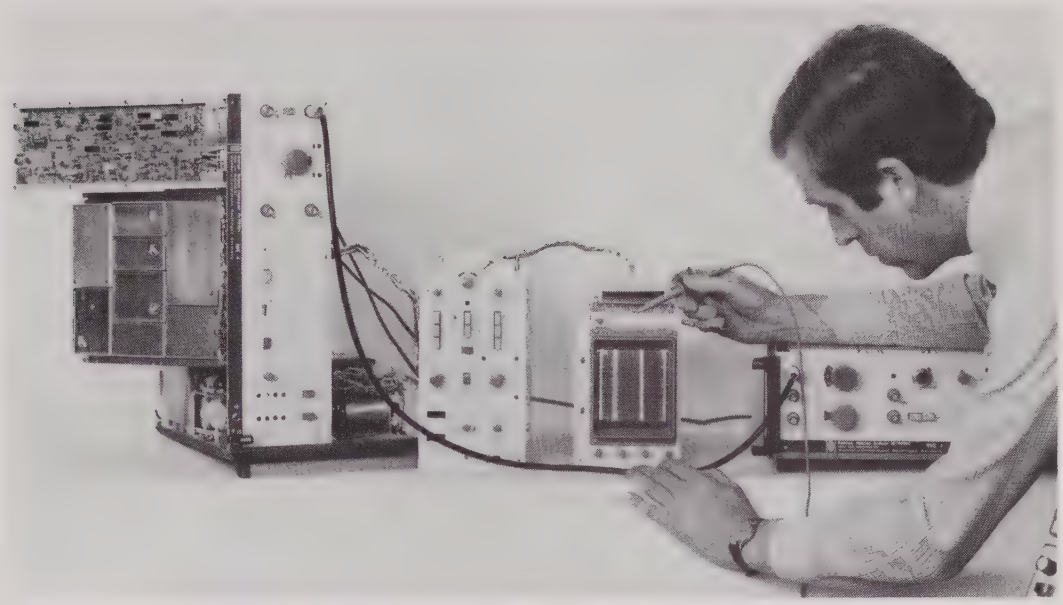


Figure 7-1: Disassembly of the RME-4 for service work

There are two hindged chassis on the underside of the lower plug-in part of the instrument. When these chassis are swung out of the way, additional circuit plates become accessible. The hinged chassis are fastened with two Phillips screws each.

The upper right plug-in part is of plug-in card construction. Access to the measuring points of the plug-in cards can be created by using the adaptor cards [697-AT] and [697-BK]. The adaptor cards can be supplied as accessories.

If required, the shielding covers on the printed circuits can be lifted off by the loops especially provided for this purpose.

Advice: When opening up the instrument and especially when disassembling it, care should be taken that the instrument is switched off and disconnected from the power supply.

7.2. Position of the Test Points, Alignment Elements and Sub-Assemblies in the Instrument

Figures 7-2 to 7-8 show the position of the test points in the instrument, which are important for trouble shooting. Furthermore, the various sub-assemblies are marked. Their identification would otherwise be difficult when the shielding cover with the plate markings is removed. The components, used for aligning, are also identified.

An instrument of the H Series was used for the photographs.

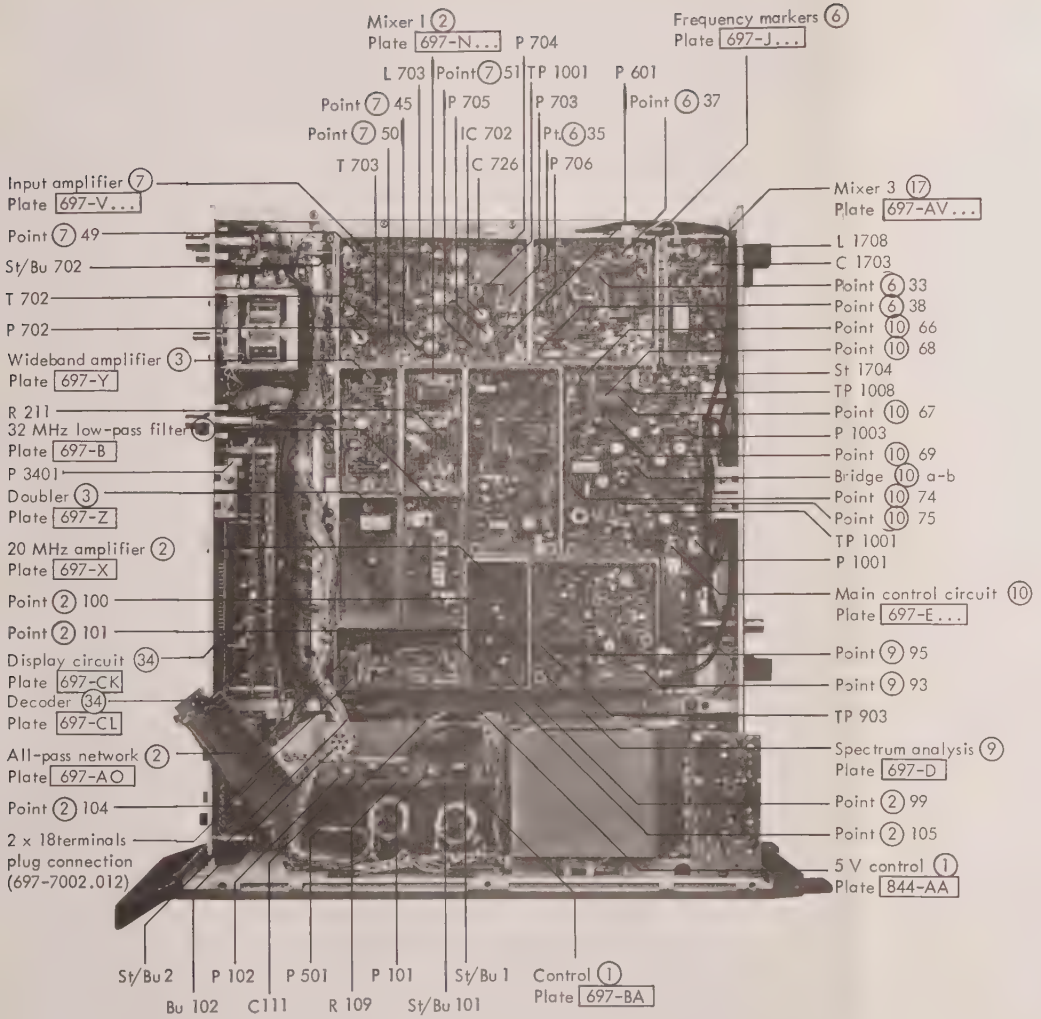


Fig. 7-2 View from above, instrument lying on the right side wall, visual part and upper right plug-in part disassembled

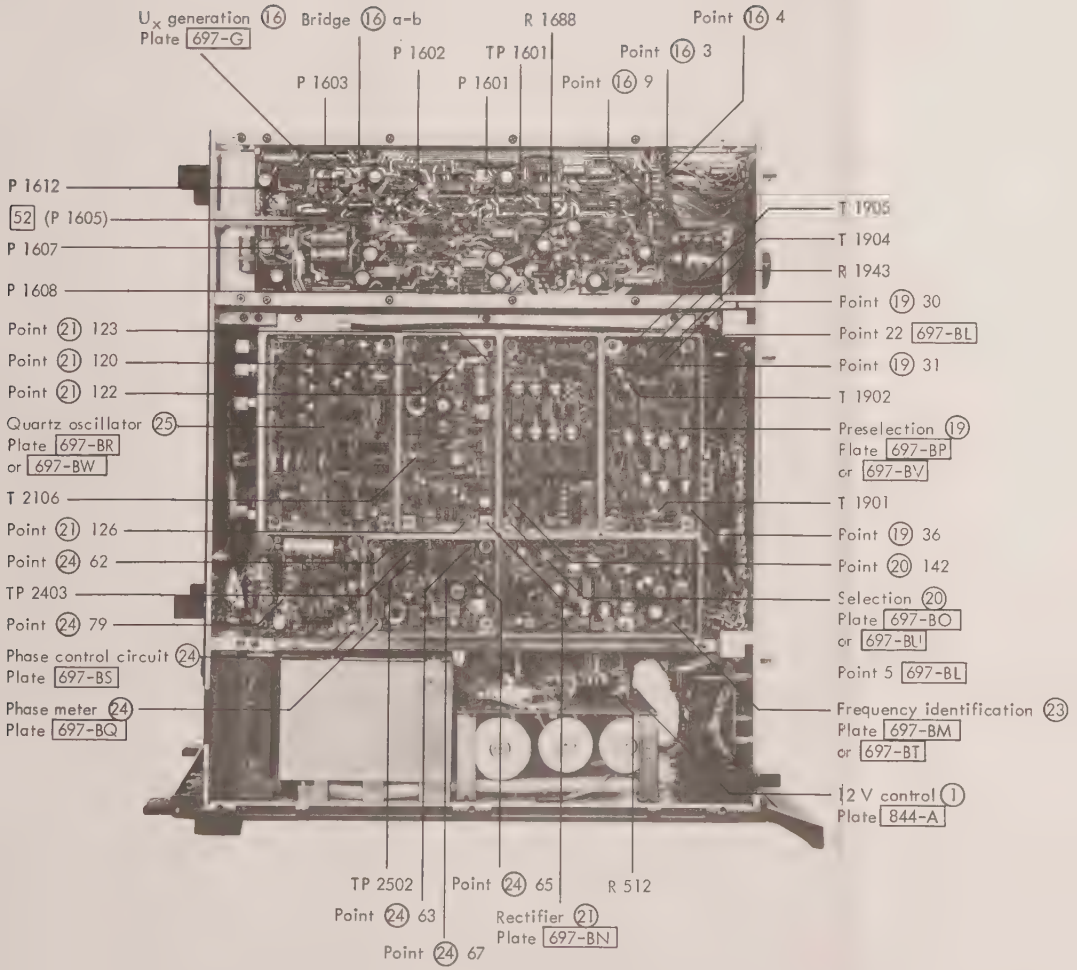


Fig. 7-3 View from below, instrument lying on the right side

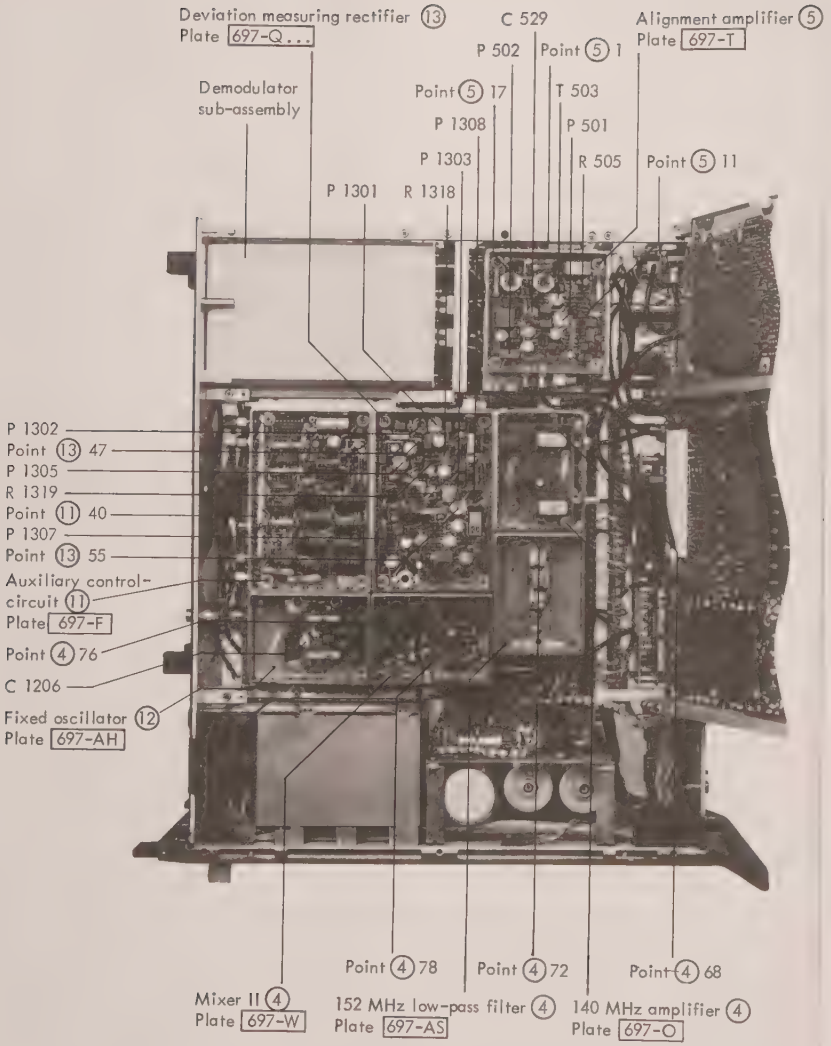


Fig. 7-4 View from below, instrument lying on the right side wall, hinged chassis swung out of the way

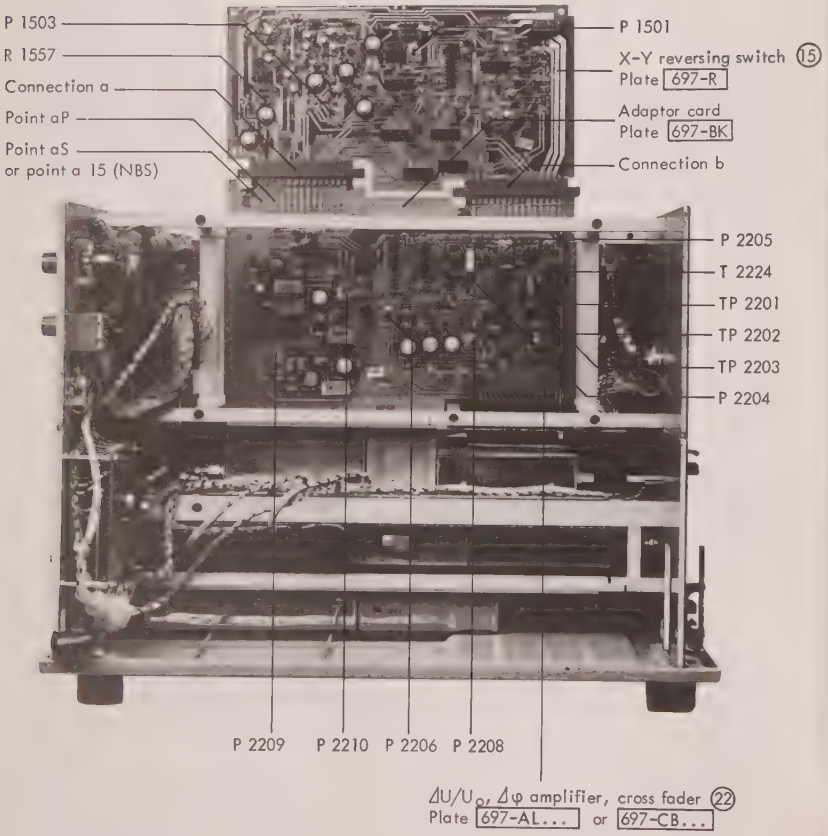


Fig. 7-5 View from the right of the plug-in cards of the sub-assembly consisting of the X-Y reversing switch (15), the $\Delta U/U_o$ amplifier, the $\Delta\varphi$ amplifier and the cross fader (22) in the upper right plug-in part, right side wall with power supply removed (NBS ≙ not inserted side)

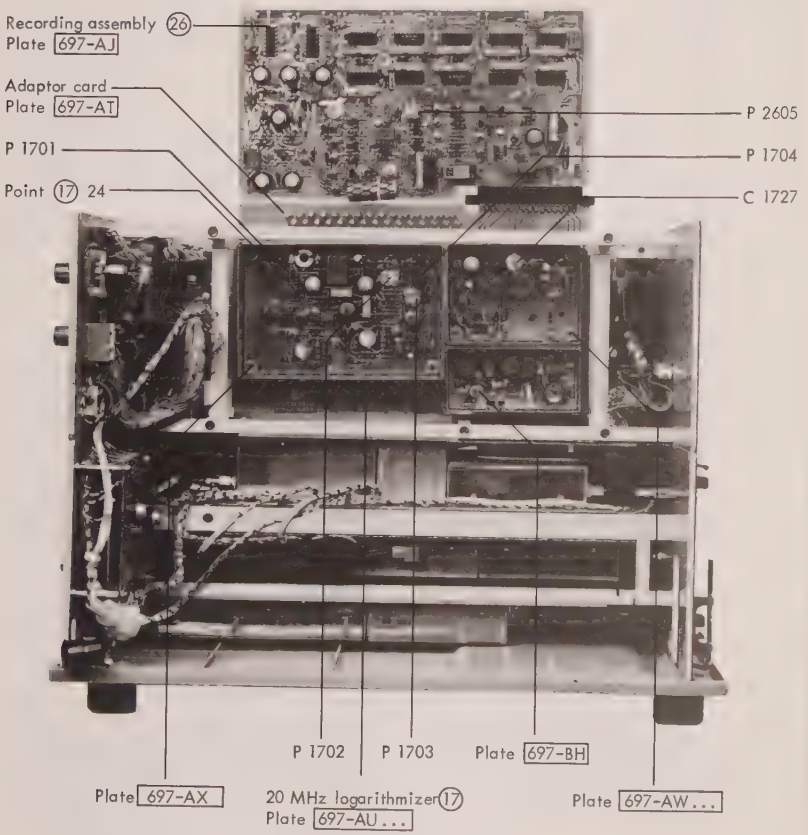


Fig. 7-6 View from the right on the plug-in cards of the recording-assembly (26) and 20 MHz logarithmizer (17) sub-assemblies in the upper right plug-in part, right side wall with power supply removed

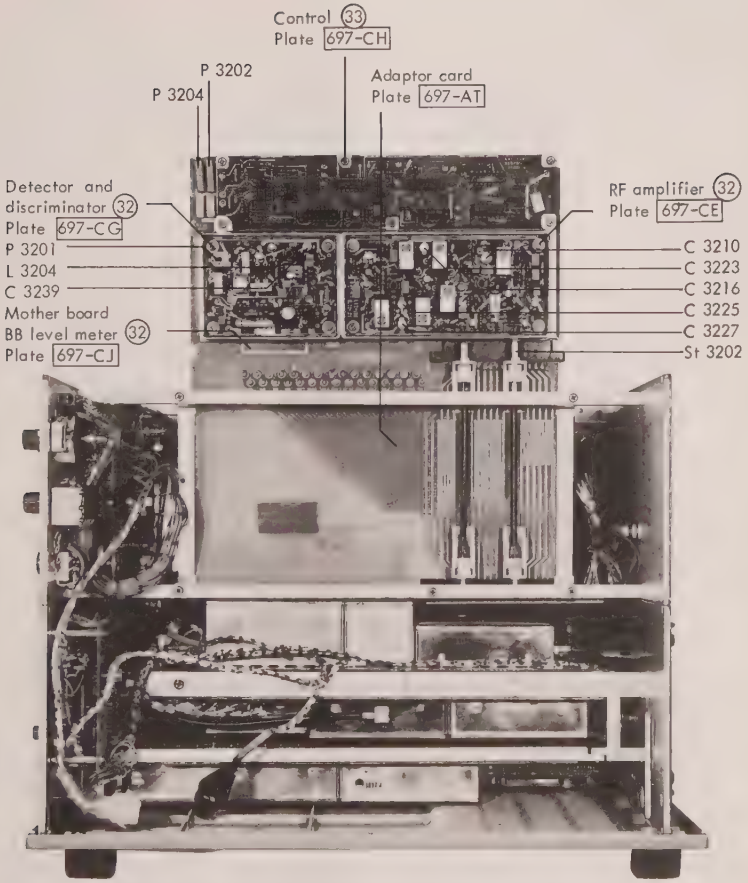


Fig. 7-6a View from right at the plug-in card of the sub-assembly BB Level Meter (32) in the upper, right partial plug-in; right side panel with power supply is removed.

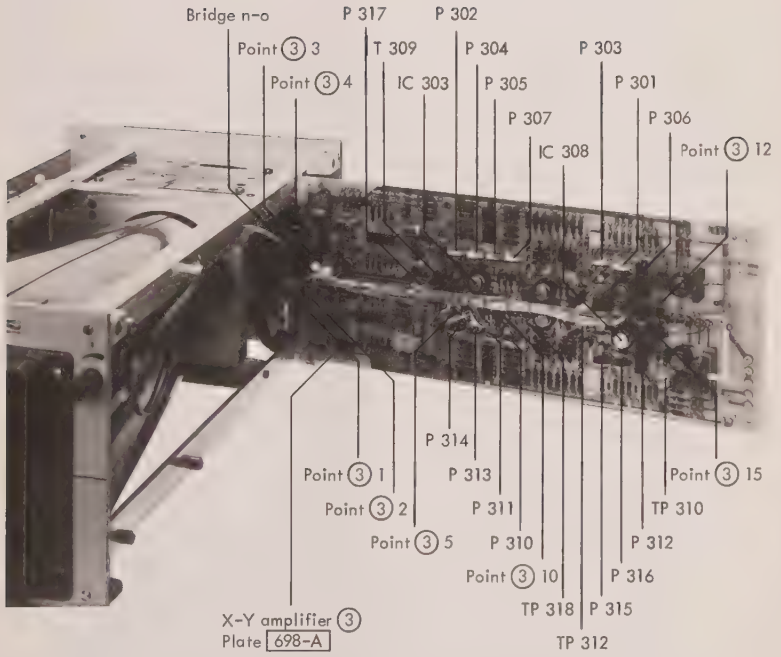


Fig. 7-7 Visual part with hinged chassis 698-A

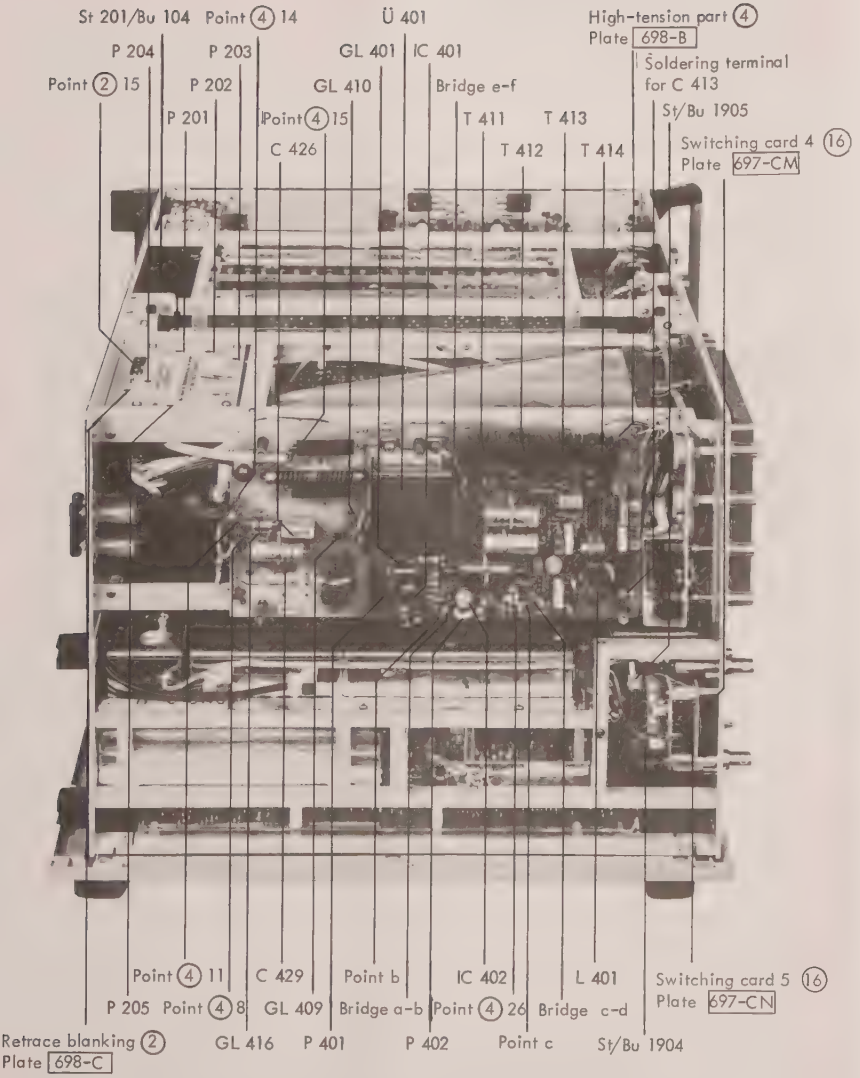


Fig. 7-8 View from the left on the visual part with the high-tension part (without protective covering)

7.3. Trouble Shooting

Trouble shooting is carried out with the help of trouble-shooting plans, which are given in Sections 7.3.2. to 7.3.15. for the most essential, conceivable defects. In addition, level plans are available for trouble shooting.

When trouble shooting, the defect, identified on the RME-4, is reproduced by a short-circuit connection between the RMS-4 and RME-4, usually by connecting the P_1 connectors. In so doing, special care should be taken to ensure that a faulty operation of the instrument has not led to a faulty behavior of the RME-4. The appropriate trouble shooting plan is then selected from a list of probable defects in Table 7-1.

Identified Defect in the RME-4	Trouble-Shooting Plan in Section
Level indicator display "too high" is lit up in spite of correct input level	7.3.2.
Level indicator display "too low" is lit up in spite of correct input level	7.3.3.
Spectrum analysis (Bessel) not possible	7.3.4.
No deviation indication	7.3.5.
No freguency markers	7.3.6.
AFC light flickers or remains dark (freguency control circuit does not catch)	7.3.7.
Measuring results are independent of input level or level indicator "two low" flickers (level control circuit does not catch)	7.3.8.
ΔP_{II} or a_r measurement not possible	7.3.9.
U_x does not synchronize or no deviation indication (defect in the X part of the RME-4; visual part removed)	7.3.10.
- all swept measurement results of 1 row of push buttons [9] or [23] or - a particular swept measurement result ΔP_I, ΔP_{II}, $\Delta\tau$ ($\Delta\varphi$), $\Delta U/U_o$ on both rows of push buttoms or - absolute levels P_I Can not be displayed	7.3.11.
No $\Delta U/U_o$ measurement results (defect in BF path)	7.3.12.
No $\Delta\tau$ or $\Delta\varphi$ measurement result (defect in BF path)	7.3.13.
Defect in display unit	7.3.14.
Error in BB level meter (Option BN 697/oo.11)	7.3.15

Table 7-1: Choosing the appropriate trouble-shooting plan

The trouble-shooting plans are used in the following manner. By checks or measurements on the instrument, an attempt is made to answer the questions posed in the individual trouble-shooting steps, with a YES or a NO. From here, one passes to the next trouble-shooting step, following the line leading upwards in the case of a YES answer and the line leading downwards in the case of a NO answer.

The measuring instruments, required for the trouble shooting, are given in the respective trouble-shooting plan.

Before commencing any trouble shooting, the DC supply voltages should be checked as described in Section 7.3.1.

7.3.1. Checking the Supply Voltages

Measuring Instrument Required:

1 digital voltmeter, e.g. the 8,000 A model of Fluke.

The DC supply voltages can be checked on the control plates 697-BA , 844-AA and 844-A of the power supply. The measurement is carried out at the measuring points given in Table 7-2.

Versorgungs-spannung	gemessen an	auf Platine	Bemerkungen
+12 V ±60 mV	R 109	697-BA	
-24 V ±48 mV	C 111 (-)	697-BA	
+5 V ±25 mV	R 512	844-AA	
+12 V ±60 mV	R 1209	844-A	Meßpunkt in den Bildern 7-2 bis 7-8 nicht erkennbar
-12 V ±60 mV	C 1215 (-)	844-A	Meßpunkt in den Bildern 7-2 bis 7-8 nicht erkennbar

Table 7-2: Checking the supply voltages

Key for Table 7-2:

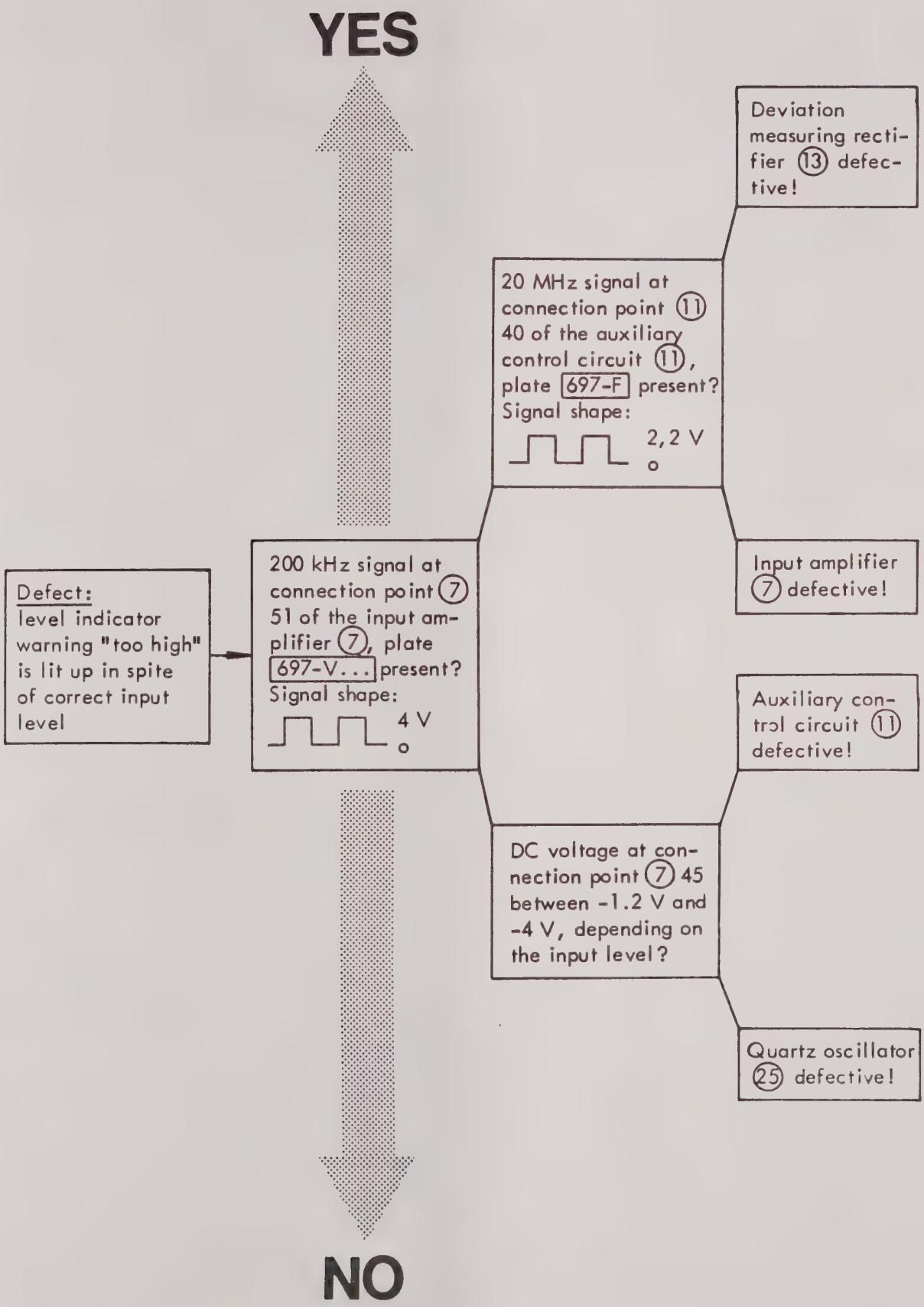
Versorgungsspannung	=	Supply voltages
gemessen an	=	Measured at
auf Platine	=	On Plate
Bemerkungen	=	Comments
Messpunkt in den Bildern...	=	Measuring point not identifiable in Figures 7-2 to 7-8

7.3.2. Trouble-shooting Plan:

Level indicator "too high" is lit up.

Measuring instruments required:

1 Digital voltmeter	e.g. 8,000 A of Fluke
1 Oscilloscope	e.g. PM-3240 of Phillips


YES
Deviation measuring rectifier (13) defective!
20 MHz signal at connection point (11) 40 of the auxiliary control circuit (11), plate 697-F present?
Signal shape:
2,2 V
o
Input amplifier (7) defective!
Defect:
level indicator warning "too high" is lit up in spite of correct input level
200 kHz signal at connection point (7) 51 of the input amplifier (7), plate 697-V... present?
Signal shape:
4 V
o
Auxiliary control circuit (11) defective!
DC voltage at connection point (7) 45 between -1.2 V and -4 V, depending on the input level?
Quartz oscillator (25) defective!
NO

7.3.3. Trouble-shooting plan: level indicator "too low" is lit up!

Measuring instruments required:

1 Digital voltmeter — e.g. 8,000 A of Fluke

1 RF millivoltmeter with VHF sensing head — e.g. 411 A with 11023 A of Hewlett Packard

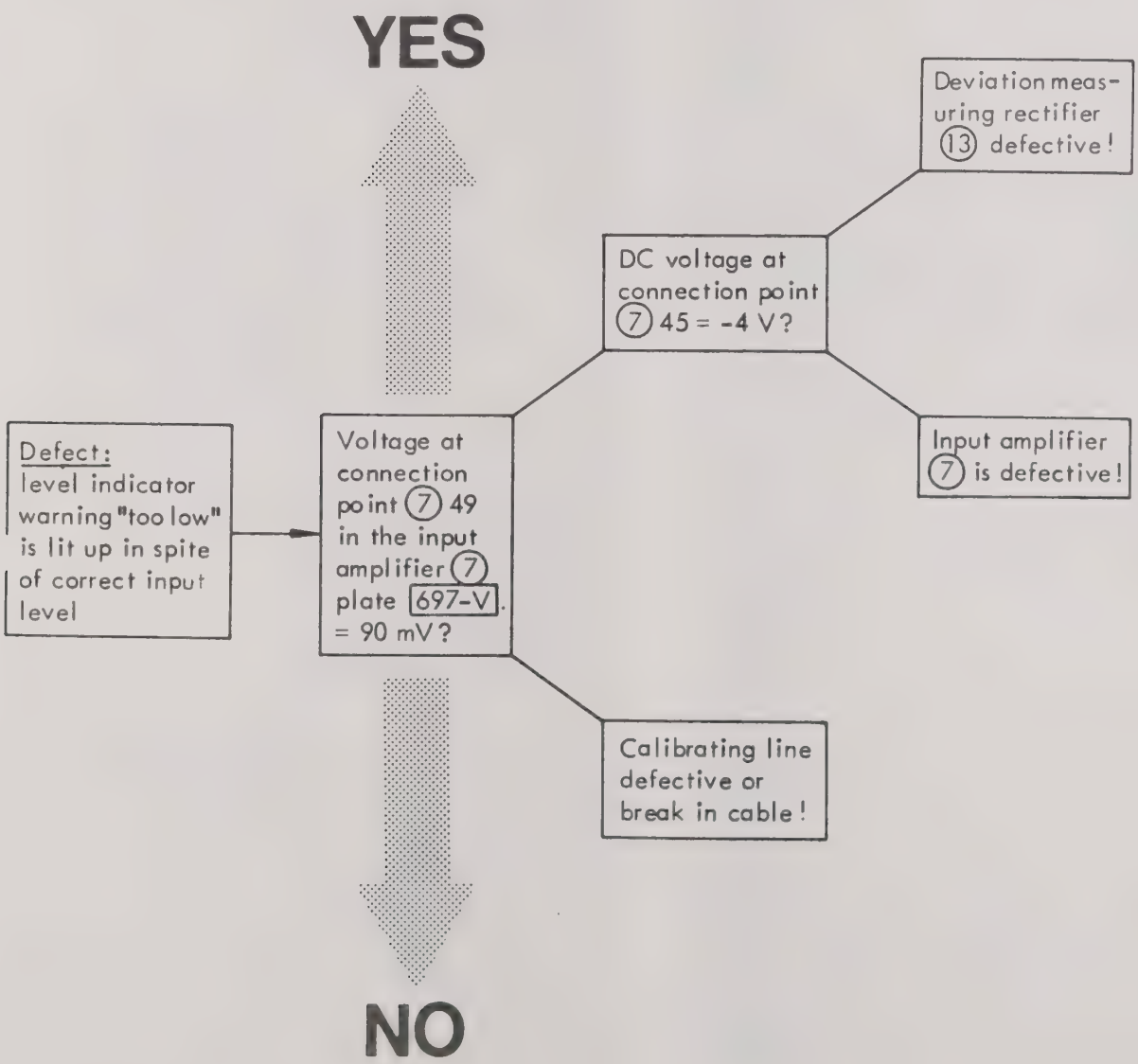
Settings of the measuring setup before starting to trouble shoot:

RMS-4: Send level 0 dBm

IF center frequency: 70 MHz

RME-4: Attenuation line 0 dBm

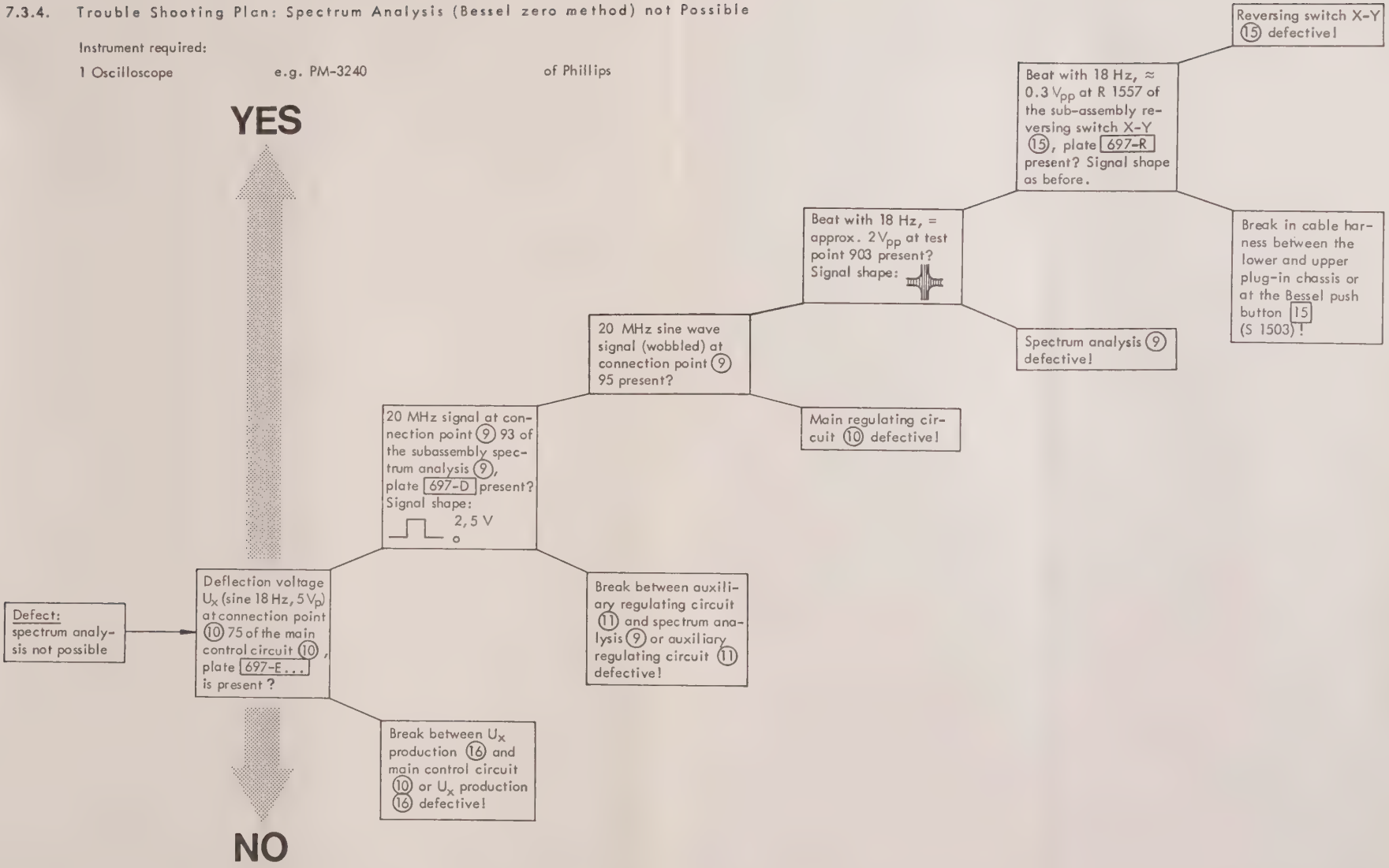
IF on 70 MHz


YES
Deviation measuring rectifier (13) defective!
DC voltage at connection point (7) 45 = -4 V?
Input amplifier (7) is defective!
Defect: level indicator warning "too low" is lit up in spite of correct input level
Voltage at connection point (7) 49 in the input amplifier (7) plate 697-V. = 90 mV?
Calibrating line defective or break in cable!
NO

7.3.4. Trouble Shooting Plan: Spectrum Analysis (Bessel zero method) not Possible

Instrument required:

1 Oscilloscope e.g. PM-3240 of Phillips


YES
NO
Defect: spectrum analysis not possible
Deflection voltage U_x (sine 18 Hz, 5 V_p) at connection point (10) 75 of the main control circuit (10), plate 697-E... is present?
Break between U_x production (16) and main control circuit (10) or U_x production (16) defective!
20 MHz signal at connection point (9) 93 of the subassembly spectrum analysis (9), plate 697-D present? Signal shape: 2,5 V o
Break between auxiliary regulating circuit (11) and spectrum analysis (9) or auxiliary regulating circuit (11) defective!
20 MHz sine wave signal (wobbled) at connection point (9) 95 present?
Main regulating circuit (10) defective!
Beat with 18 Hz, = approx. 2 V_{pp} at test point 903 present? Signal shape:
Spectrum analysis (9) defective!
Beat with 18 Hz, ≈ 0.3 V_{pp} at R 1557 of the sub-assembly reversing switch X-Y (15), plate 697-R present? Signal shape as before.
Break in cable harness between the lower and upper plug-in chassis or at the Bessel push button 15 (S 1503)!
Reversing switch X-Y (15) defective!

7.3.5. Trouble Shooting Plan: No Deviation Indication

Instruments required:

1 Oscilloscope	e.g. PM 3240	of Philips
1 RF millivoltmeter with sensing head	e.g. 411 A with 11023 A	of Hewlett Packard
1 Digital voltmeter	e.g. 8000A	of Fluke

Setting at the measuring set-up before starting to troubleshoot:

RMS-4: Lower measuring frequency 0.093 (0.083) MHz or 0.277 (0.25) MHz

Test deviation Δf to 500 kHz

IF center frequency 70 MHz

Sweep deviation $\hat{\Delta F}$ to null

RME-4: Tracking operation

IF to 70 MHz

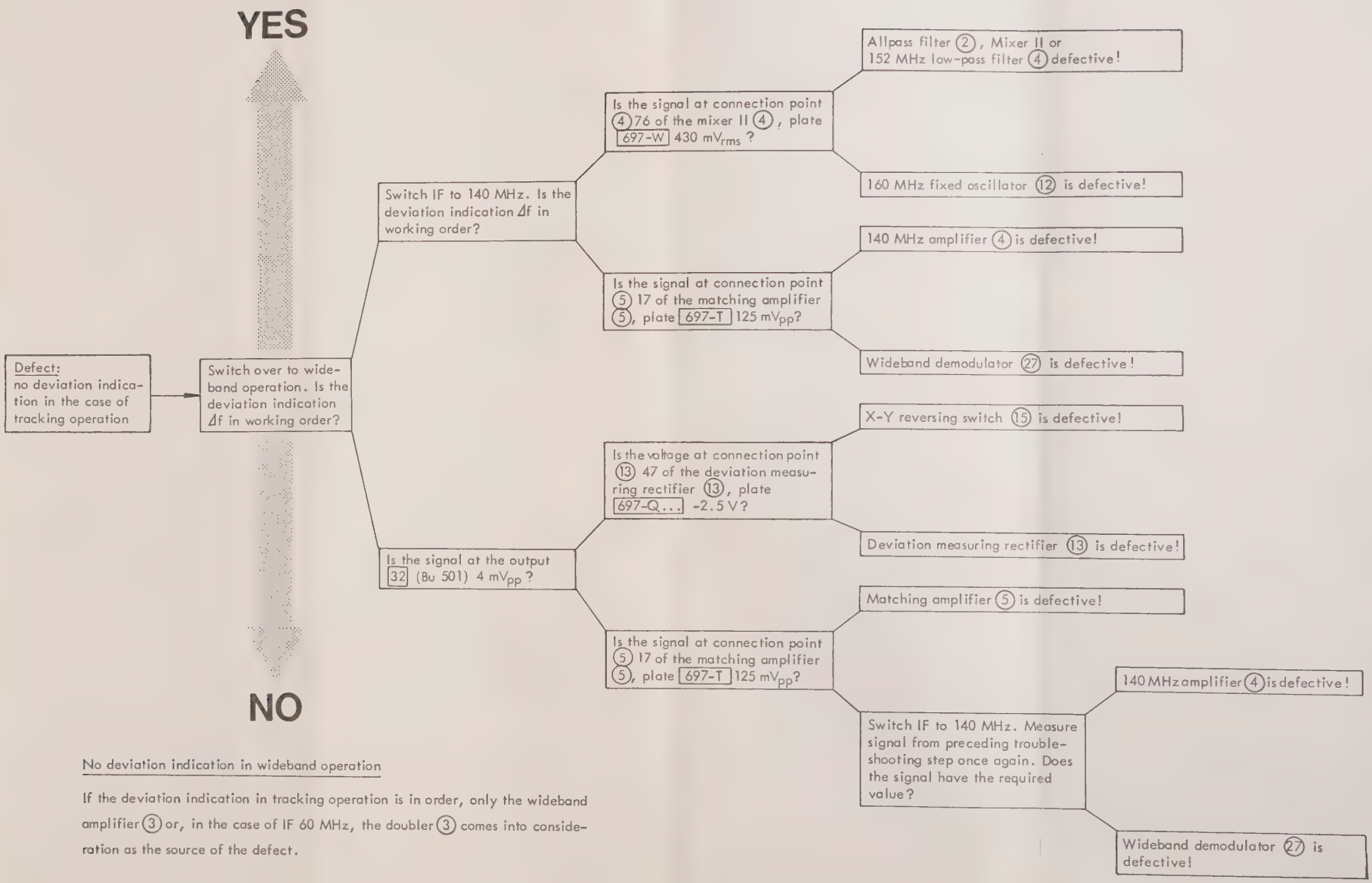
Push button 15 "Δf, P_i" depressed

Precondition for the trouble shooting:

Level indicators GI 1303 "too low" and GI 1304 "too high" not lit up.

AFC light GI 1007 lit up

Advice: See also trouble shooting plan in Section 7.3.10.


YES
NO
Defect:
no deviation indication in the case of tracking operation
Switch over to wideband operation. Is the deviation indication Δf in working order?
Switch IF to 140 MHz. Is the deviation indication Δf in working order?
Is the signal at connection point (4) 76 of the mixer II (4), plate 697-W 430 mVrms ?
Allpass filter (2), Mixer II or 152 MHz low-pass filter (4) defective!
160 MHz fixed oscillator (12) is defective!
Is the signal at connection point (5) 17 of the matching amplifier (5), plate 697-T 125 mVpp?
140 MHz amplifier (4) is defective!
Wideband demodulator (27) is defective!
Is the signal at the output 32 (Bu 501) 4 mVpp ?
Is the voltage at connection point (13) 47 of the deviation measuring rectifier (13), plate 697-Q... -2.5 V?
X-Y reversing switch (15) is defective!
Deviation measuring rectifier (13) is defective!
Is the signal at connection point (5) 17 of the matching amplifier (5), plate 697-T 125 mVpp?
Matching amplifier (5) is defective!
Switch IF to 140 MHz. Measure signal from preceding troubleshooting step once again. Does the signal have the required value?
140 MHz amplifier (4) is defective!
Wideband demodulator (27) is defective!

No deviation indication in wideband operation

If the deviation indication in tracking operation is in order, only the wideband amplifier (3) or, in the case of IF 60 MHz, the doubler (3) comes into consideration as the source of the defect.

7.3.6. Trouble Shooting Plan: No Frequency Markers

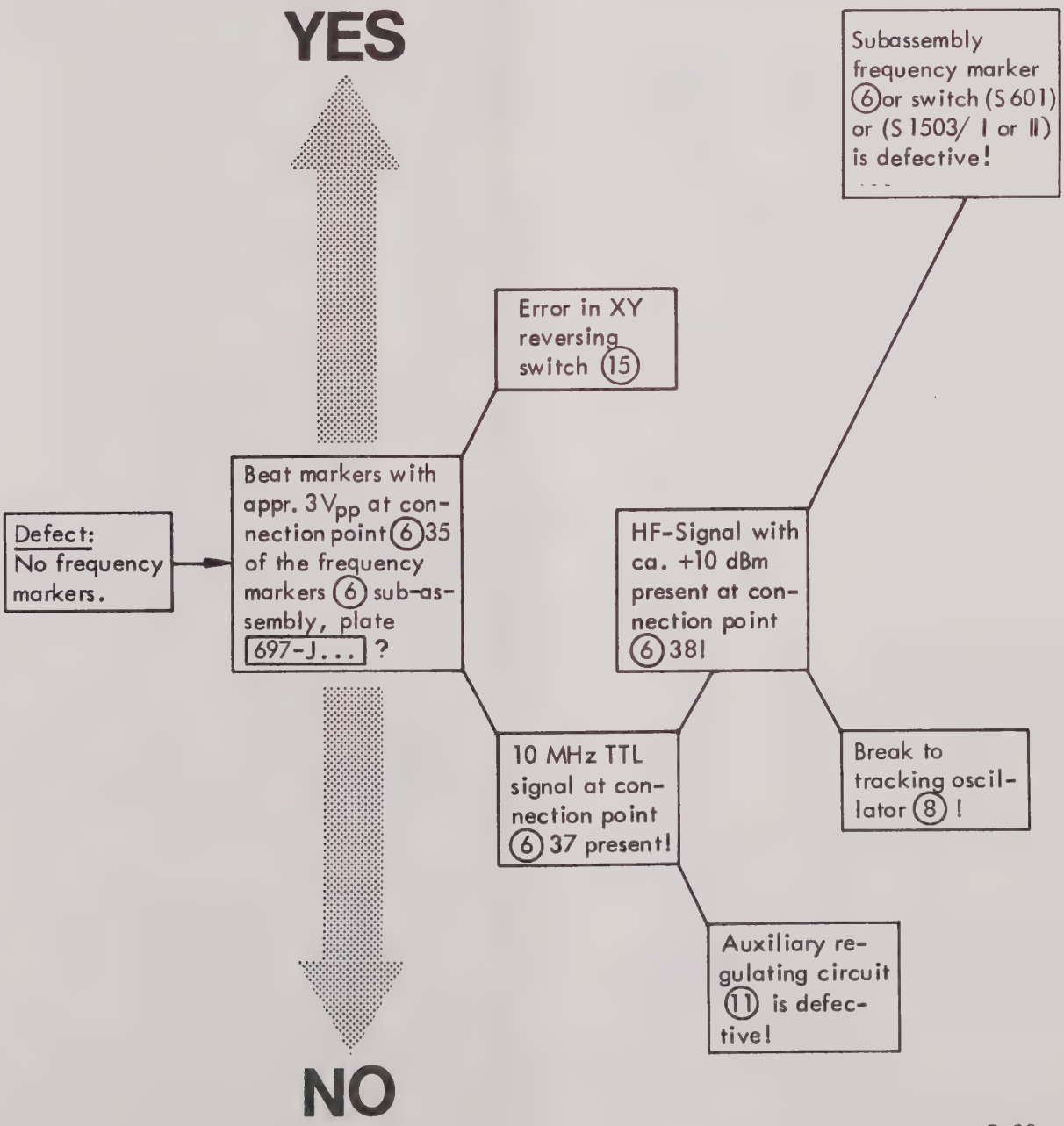
Instruments required:

1 Oscilloscope	e.g. PM 3240	of Philips
1 RF millivoltmeter with VHF sensing head	e.g. 411 A with 11023 A	of Hewlett Packard

Precondition for the Trouble Shooting:

Level indicators GI 1304 "too high" and GI 1303 "too low" not lit up.

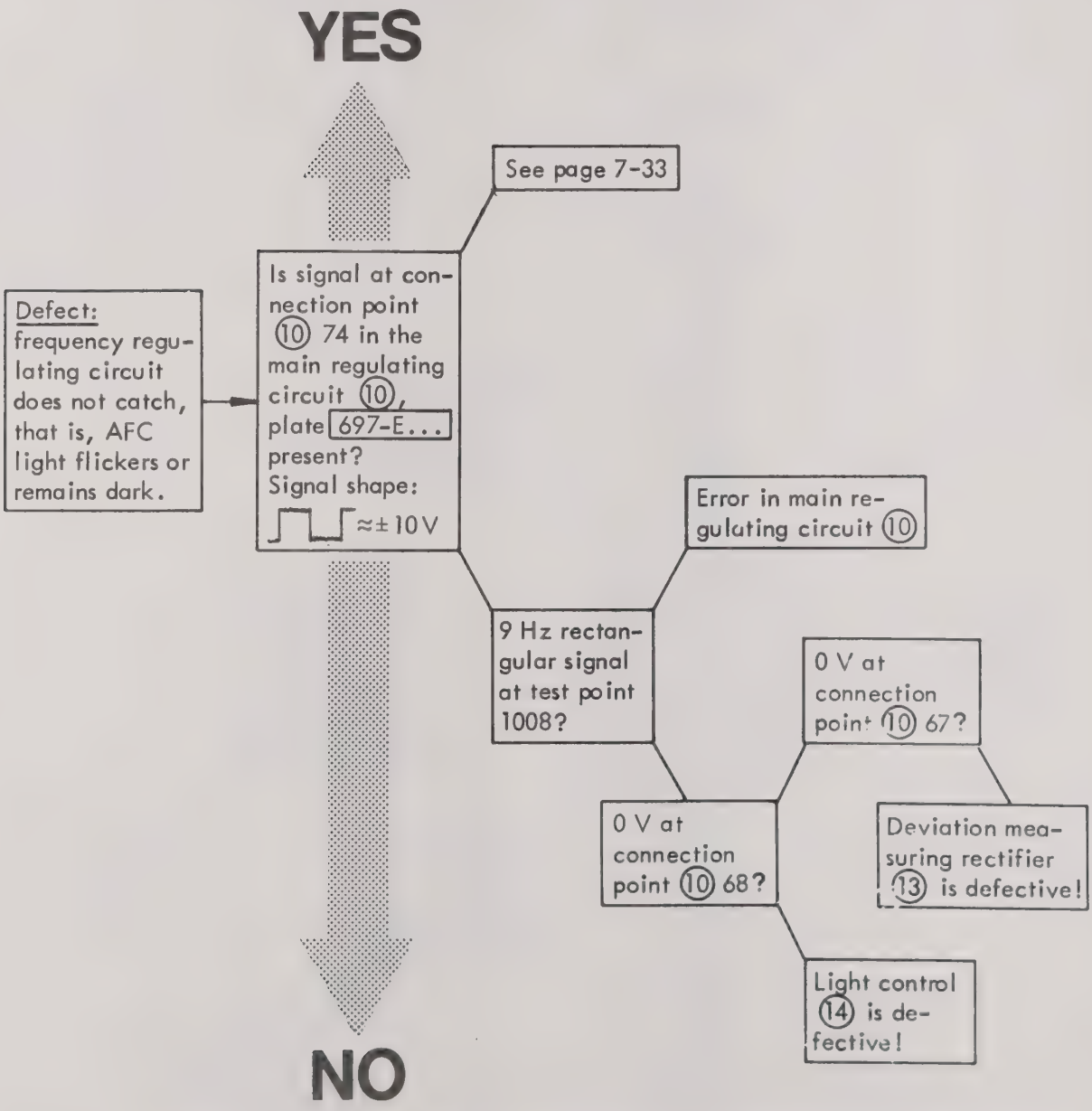
AFC light GI 1007 lit up.


YES
Subassembly frequency marker (6) or switch (S 601) or (S 1503/ I or II) is defective!
Error in XY reversing switch (15)
Beat markers with appr. 3 Vpp at connection point (6) 35 of the frequency markers (6) sub-assembly, plate 697-J... ?
Defect: No frequency markers.
HF-Signal with ca. +10 dBm present at connection point (6) 38!
10 MHz TTL signal at connection point (6) 37 present!
Break to tracking oscillator (8) !
Auxiliary regulating circuit (11) is defective!
NO

7.3.7. Trouble Shooting Plan: Frequency Regulating Circuit does not catch

Instruments required:

1 Frequency counter (to 35 MHz)	e.g. 5382 A	of Hewlett Packard
1 Oscilloscope	e.g. 3240	of Philips
1 RF millivoltmeter with VHF sensing head	e.g. 411 A with 11023 A	of Hewlett Packard


YES
See page 7-33
Defect:
frequency regulating circuit does not catch, that is, AFC light flickers or remains dark.
Is signal at connection point (10) 74 in the main regulating circuit (10), plate 697-E... present?
Signal shape:
≈±10V
Error in main regulating circuit (10)
9 Hz rectangular signal at test point 1008?
0 V at connection point (10) 67?
0 V at connection point (10) 68?
Deviation measuring rectifier (13) is defective!
Light control (14) is defective!
NO

It helps in trouble shooting if mutually interaction frequency and level regulating circuits are kept in a defined state.

Fixing Frequency Regulating Circuit: Connection point (10) 74 on plate [697-E...] on chassis

Fixing Level Regulating Circuit: Change soldering position of bridge (16) a-b on plate [697-G] to (16) a-c

- At connection point (7) 50 on plate [697-V...] of the input amplifier (7) adjust to 125±25mV with the help of the IF fine level adjustment (2) of the RMS-4. Use millivoltmeter.

- At connection point (2) 100, plate [697-X] of the 20 MHz amplifier, there must be ca. 90 mV, and at connection point (2) 101 350±70mV.

Through fixing the frequency regulating circuit, the tracking oscillator (8) oscillates at 90 MHz or 160 MHz, depending on the IF selected.

The If at connection point (2) 99, plate [697-X] of the 20 MHz amplifier is measured with a frequency counter (possible an oscilloscope) and adjusted with the potentiometer (3) at the RMS-4 (at the same time, switch [4] is in the position "IF shift") according to the following trouble shooting steps.

- Adjust send frequency in such a way, that the IF is about 33 MHz.

  a) With the oscilloscope, measure voltage at connection point (10) 69, plate [697-E...] of the main regulating circuit (10). Nominal value > 3V.
  If V < 3V, then the spectrum analysis sub-assembly (3) is defective!

b) At connection point (10) 66, measure O V signal. If there are impulses, defect is in auxiliary regulating circuit (11) !

- Change send frequency in such a way, that the IF at connection point (2) 99 in the 20 MHz amplifier (2) = approximately 25 MHz.

- The voltage at connection point (10) 69 of the main regulating circuit must be <0.5 V, otherwise spectrum anaylsis sub-assembly (9) is defective!

- Change send frequency in such a way, that the IF at connection point (2) 99 in the 20 MHz amplifier (2) = approximately 15 MHz. At connection point (10) 66, measure TTL signals with an impulse width of ca. 400 ns. If these are not measurable, defect is in auxiliary regulating circuit (11) !.

Otherwise, defect is in main regulating circuit (10) !

7.3.8. Trouble Shooting Plan: Level regulating circuit does not catch

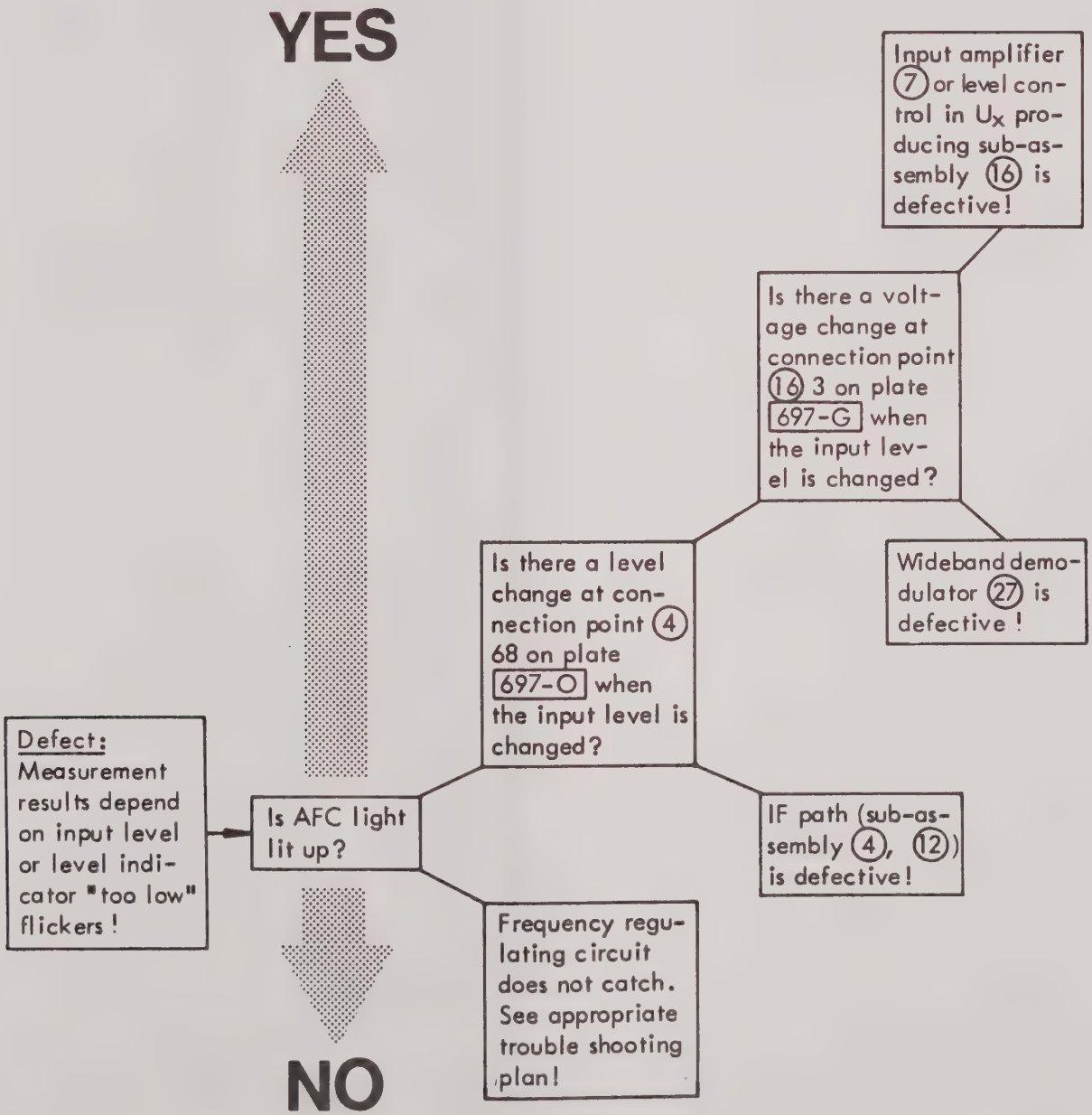
Instrument required:

1 RF millivoltmeter with VHF sensing head	e.g. 411 A with 11023 A	of Hewlett Packard

Precondition for the trouble shooting:

IF input level ca. -10 dBm

Change soldering position of bridge (16) a-b on plate [697-G] of the U_x producing sub-assembly (16) to (16) a-c.


YES
Input amplifier (7) or level control in Ux producing sub-assembly (16) is defective!
Is there a voltage change at connection point (16) 3 on plate [697-G] when the input level is changed?
Wideband demodulator (27) is defective!
Is there a level change at connection point (4) 68 on plate [697-O] when the input level is changed?
IF path (sub-assembly (4), (12)) is defective!
Defect: Measurement results depend on input level or level indicator "too low" flickers!
Is AFC light lit up?
Frequency regulating circuit does not catch. See appropriate trouble shooting plan!
NO

Check Input Amplifier: Sever bridge (16) a-b or (16) a-c on plate [697-G] of the U_x producing sub-assembly (16).

By changing the input level from -20 to -10 dBm, the level at connection point (7) 50 (plate [697-V...]) can be kept constant at 120 mV by a DC voltage at connection point (16) a in the range of 0 to -5 V.

7.3.9. Trouble Shooting Plan: ΔP_{11} or a_r measurement not possible

Instruments required:

1 Frequency counter	e.g. FZ-4	of W&G
1 Selective level meter with sensing head	e.g. SPM-14	of W&G

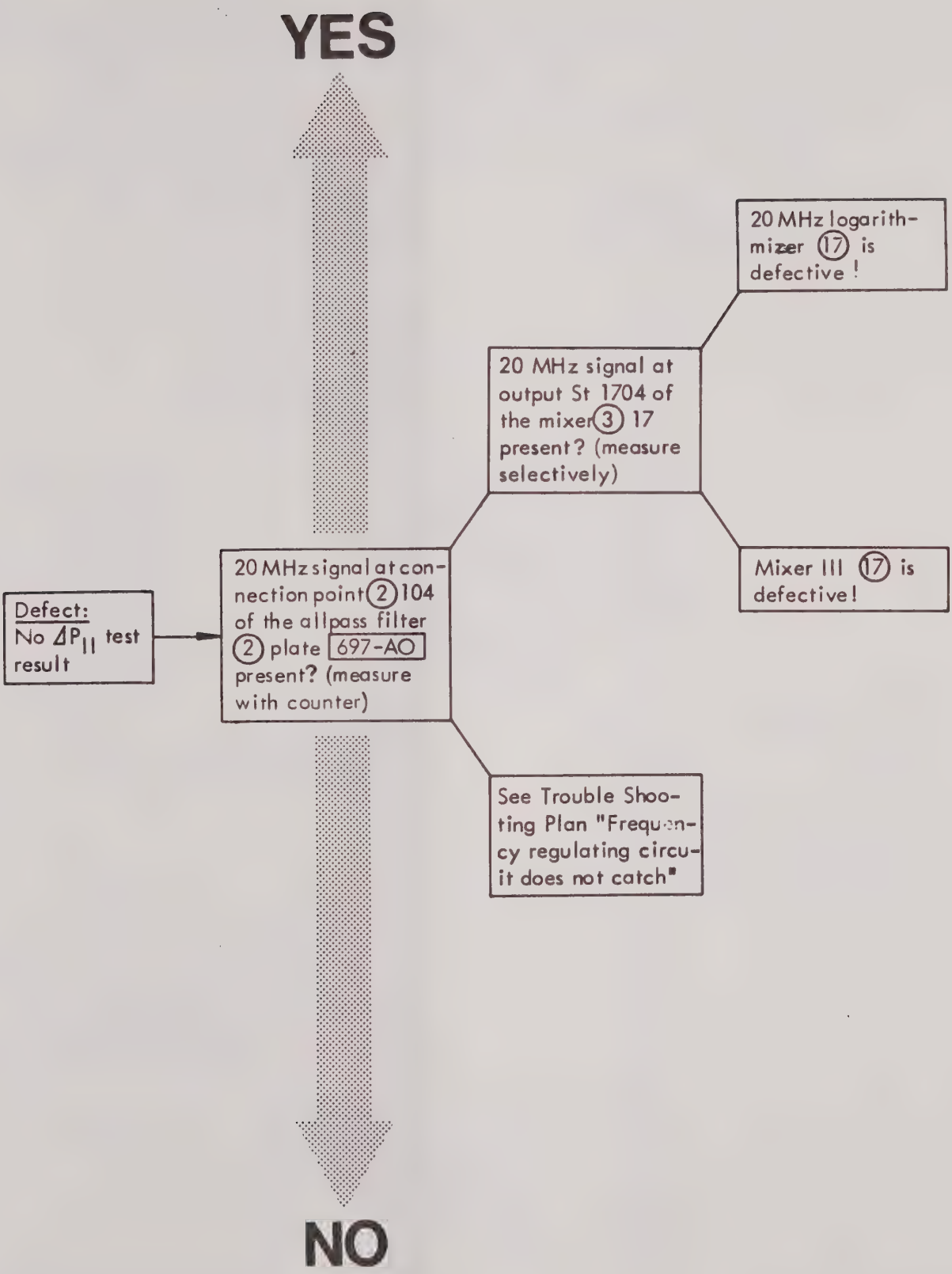
Test construction for the trouble shooting:

Back-to-back connection between RMS output [1] (Bu 1) and RME input [28] (Bu 1701)

Back-to-back connection between RMS output [10] (Bu 502) and RME input [27] (Bu 1)

P_1 send level at RMS-4: <-10 dBm!

Sweep or tracking operation!

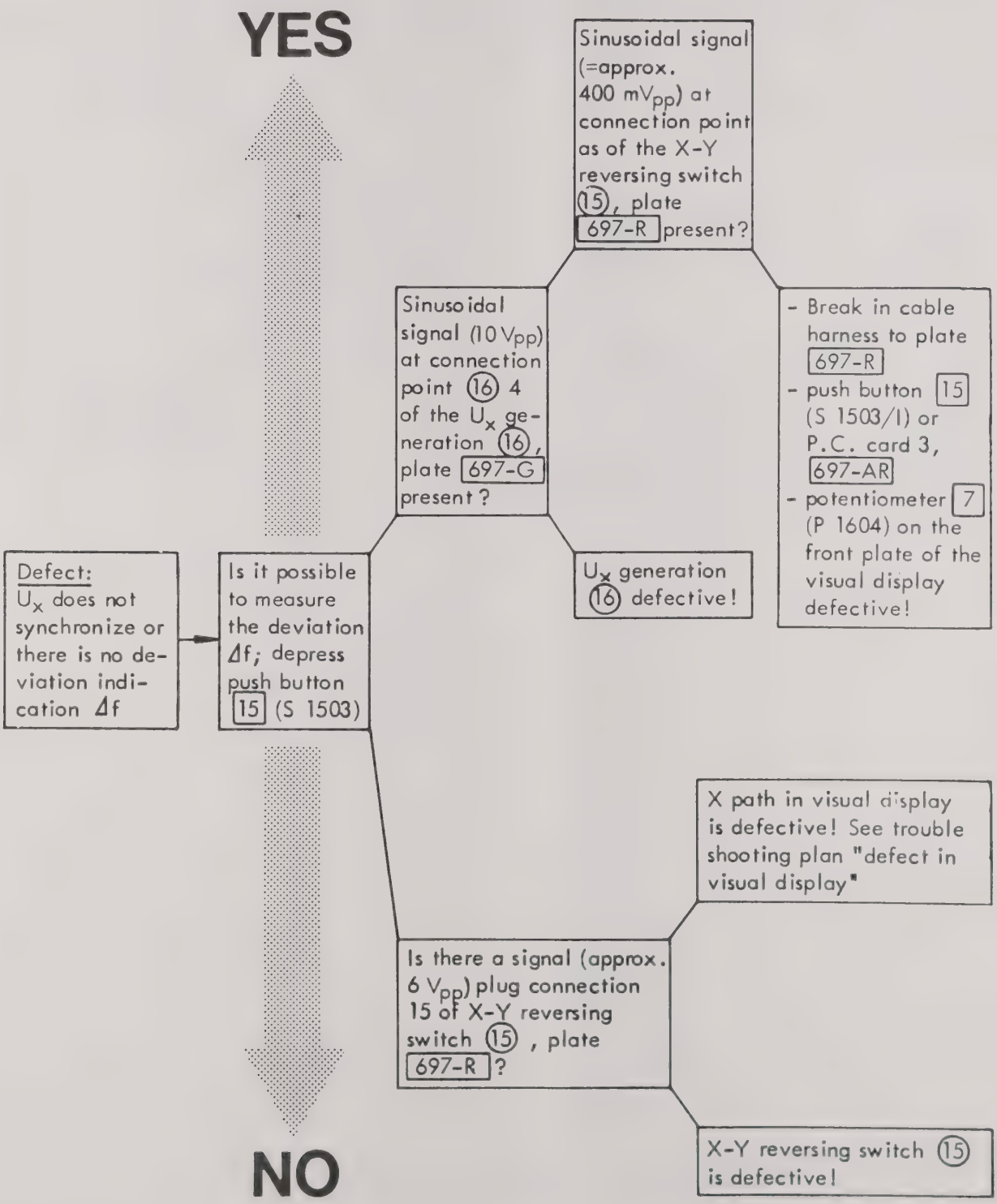

YES
20 MHz logarithmizer (17) is defective !
20 MHz signal at output St 1704 of the mixer (3) 17 present? (measure selectively)
Mixer III (17) is defective!
Defect: No ΔP_{II} test result
20 MHz signal at connection point (2) 104 of the allpass filter (2) plate 697-AO present? (measure with counter)
See Trouble Shooting Plan "Frequency regulating circuit does not catch"
NO

Advice: See also Trouble Shooting Plan in Section 7.3.11.

7.3.10. Trouble Shooting Plan: Defect in X path (without display unit)

Instruments required:

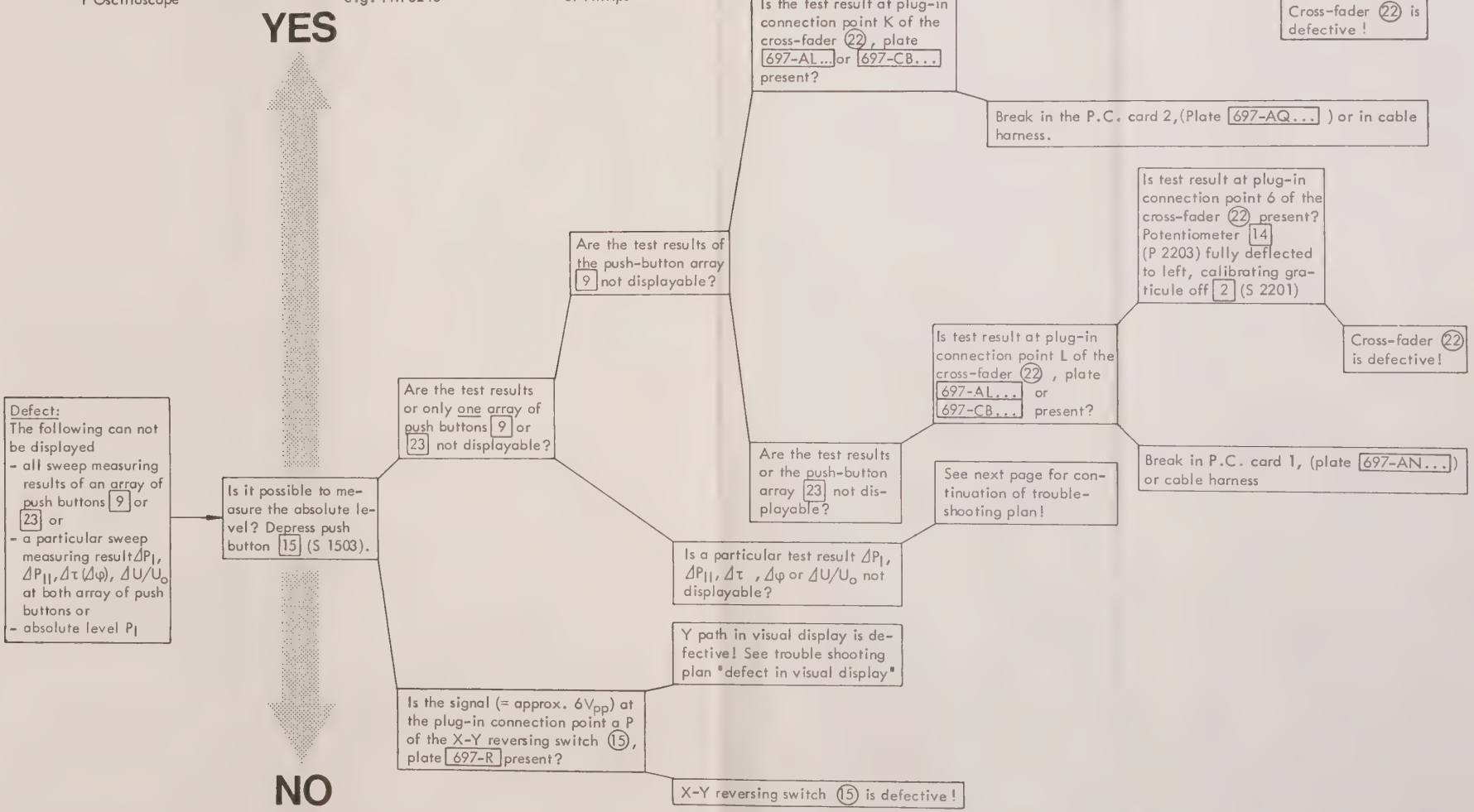
1 Oscilloscope e.g. PM 3240 of Philips

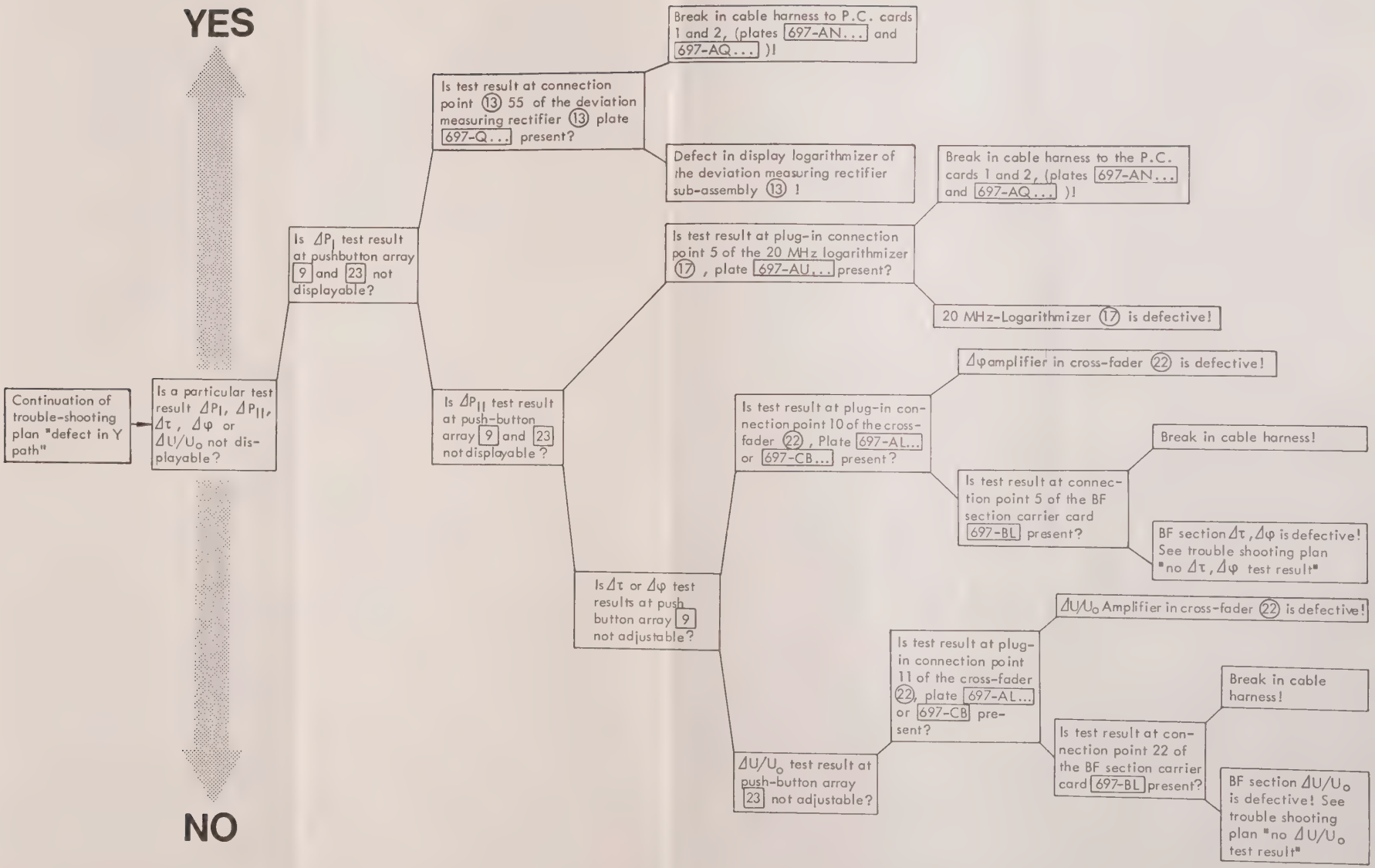

YES
Defect: U_x does not synchronize or there is no deviation indication Δf
Is it possible to measure the deviation Δf; depress push button 15 (S 1503)
Sinusoidal signal (=approx. 400 mV_{pp}) at connection point as of the X-Y reversing switch (15), plate 697-R present?
Sinusoidal signal (10 V_{pp}) at connection point (16) 4 of the U_x generation (16), plate 697-G present?
- Break in cable harness to plate 697-R
- push button 15 (S 1503/1) or P.C. card 3, 697-AR
- potentiometer 7 (P 1604) on the front plate of the visual display defective!
U_x generation (16) defective!
X path in visual display is defective! See trouble shooting plan "defect in visual display"
Is there a signal (approx. 6 V_{pp}) plug connection 15 of X-Y reversing switch (15), plate 697-R ?
X-Y reversing switch (15) is defective!
NO

7.3.11. Trouble Shooting Plan: Defect in Y path (without visual display)

Instrument required:

1 Oscilloscope e.g. PM 3240 of Philips


YES
NO
Defect:
The following can not be displayed
- all sweep measuring results of an array of push buttons 9 or 23 or
- a particular sweep measuring result ΔP_I, ΔP_II, Δτ (Δφ), ΔU/U_o at both array of push buttons or
- absolute level P_I
Is it possible to measure the absolute level? Depress push button 15 (S 1503).
Are the test results or only one array of push buttons 9 or 23 not displayable?
Are the test results of the push-button array 9 not displayable?
Is the test result at plug-in connection point K of the cross-fader 22, plate 697-AL... or 697-CB... present?
Is test result at plug-in connection point 6 of the cross-fader 22 present? Potentiometer 14 (P 2203) fully deflected to right, calibration graticule off 2 (S 2201)
Cross-fader 22 is defective !
Break in the P.C. card 2, (Plate 697-AQ...) or in cable harness.
Are the test results or the push-button array 23 not displayable?
Is test result at plug-in connection point L of the cross-fader 22, plate 697-AL... or 697-CB... present?
Is test result at plug-in connection point 6 of the cross-fader 22 present? Potentiometer 14 (P 2203) fully deflected to left, calibrating graticule off 2 (S 2201)
Cross-fader 22 is defective!
Break in P.C. card 1, (plate 697-AN...) or cable harness
Is a particular test result ΔP_I, ΔP_II, Δτ, Δφ or ΔU/U_o not displayable?
See next page for continuation of trouble-shooting plan!
Y path in visual display is defective! See trouble shooting plan "defect in visual display"
Is the signal (= approx. 6V_pp) at the plug-in connection point a P of the X-Y reversing switch 15, plate 697-R present?
X-Y reversing switch 15 is defective !


YES
NO
Continuation of trouble-shooting plan "defect in Y path"
Is a particular test result ΔP_I, ΔP_{II}, $\Delta\tau$, $\Delta\varphi$ or $\Delta U/U_o$ not displayable?
Is ΔP_I test result at pushbutton array 9 and 23 not displayable?
Is ΔP_{II} test result at push-button array 9 and 23 not displayable?
Is test result at connection point (13) 55 of the deviation measuring rectifier (13) plate 697-Q... present?
Break in cable harness to P.C. cards 1 and 2, (plates 697-AN... and 697-AQ...)!
Defect in display logarithmizer of the deviation measuring rectifier sub-assembly (13) !
Is test result at plug-in connection point 5 of the 20 MHz logarithmizer (17) , plate 697-AU... present?
Break in cable harness to the P.C. cards 1 and 2, (plates 697-AN... and 697-AQ...)!
20 MHz-Logarithmizer (17) is defective!
Is $\Delta\tau$ or $\Delta\varphi$ test results at push button array 9 not adjustable?
Is test result at plug-in connection point 10 of the cross-fader (22) , Plate 697-AL... or 697-CB... present?
$\Delta\varphi$ amplifier in cross-fader (22) is defective!
Is test result at connection point 5 of the BF section carrier card 697-BL present?
Break in cable harness!
BF section $\Delta\tau$, $\Delta\varphi$ is defective! See trouble shooting plan "no $\Delta\tau$, $\Delta\varphi$ test result"
$\Delta U/U_o$ test result at push-button array 23 not adjustable?
Is test result at plug-in connection point 11 of the cross-fader (22), plate 697-AL... or 697-CB present?
$\Delta U/U_o$ Amplifier in cross-fader (22) is defective!
Is test result at connection point 22 of the BF section carrier card 697-BL present?
Break in cable harness!
BF section $\Delta U/U_o$ is defective! See trouble shooting plan "no $\Delta U/U_o$ test result"

7.3.12. Trouble Shooting Plan: No $\Delta U/U_o$ Test Result (defect in BF path)

Instruments required:

1 RF millivoltmeter with VHF sensing head	e.g. 411 A with 11023 A	of Hewlett Packard
1 Oscilloscope	e.g. PM 3240	of Philips

Adjustments of measuring setup before starting to trouble shoot:

RMS-4: Test frequency 250 or 277.77 kHz

Test voltage -20 dBm/-40 dBm ←

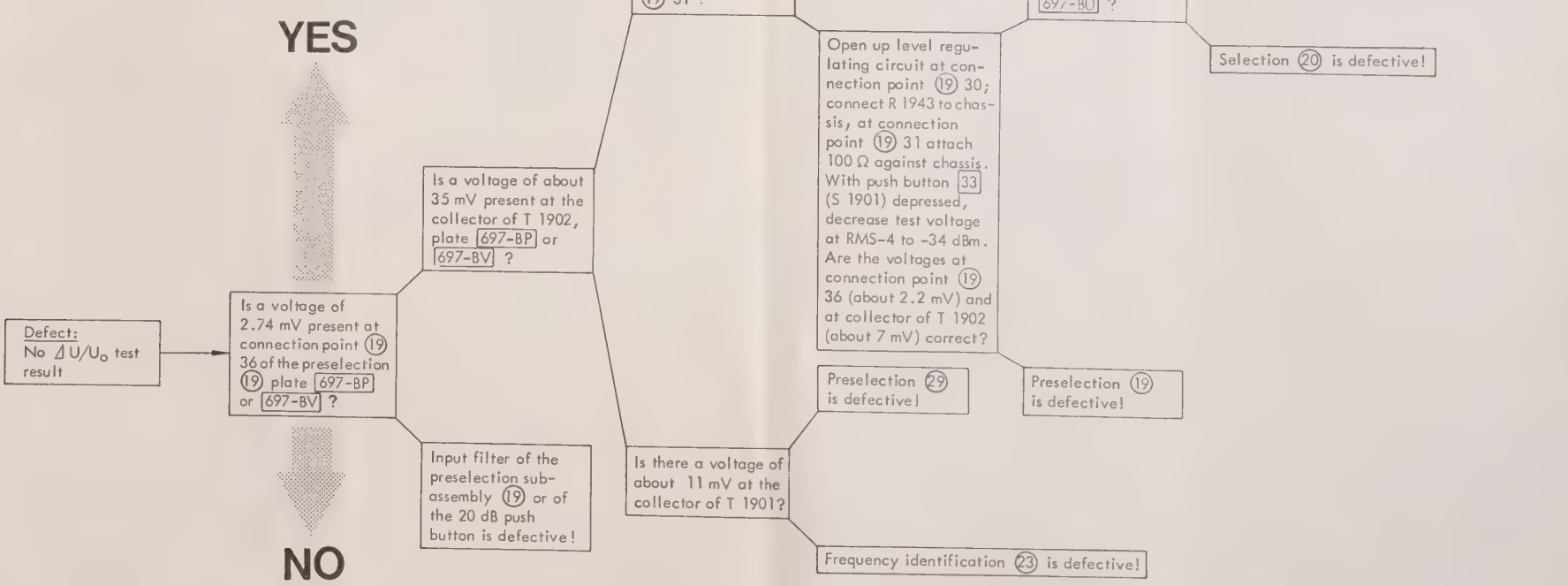
Sweep voltage to 0 V

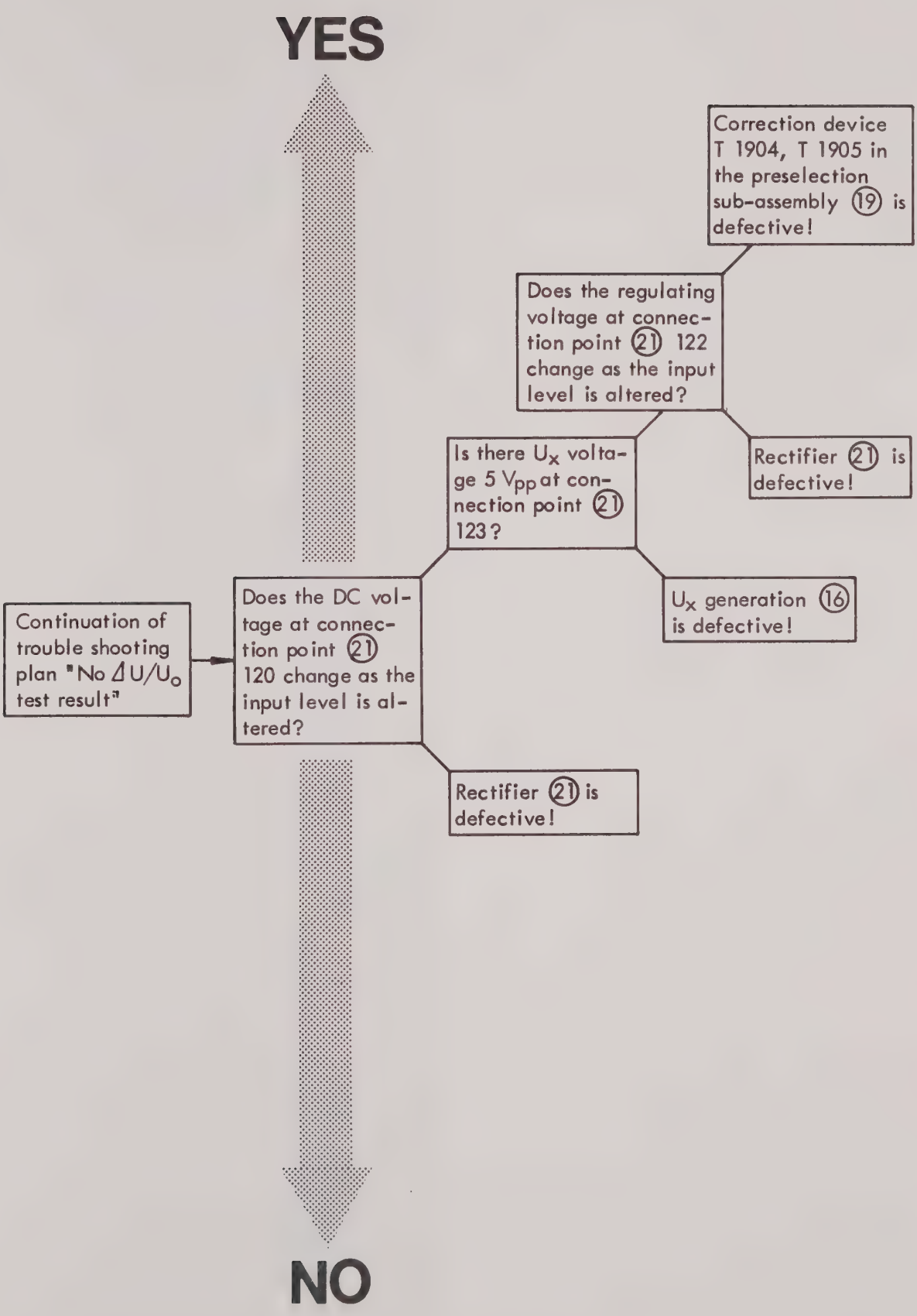
RME-4: Switch [29] (S 1601) to BF

Push button [33] (S 1901) depressed/not depressed ←

$\Delta U/U_o$ push button at [23] (S 2204) actuated

Back-to-back connection between RMS-output [14] (Bu 1605) and RME-input [30] (Bu 1901)


Defect: No $\Delta U/U_o$ test result
Is a voltage of 2.74 mV present at connection point (19) 36 of the preselection (19) plate [697-BP] or [697-BV] ?
YES
NO
Is a voltage of about 35 mV present at the collector of T 1902, plate [697-BP] or [697-BV] ?
Input filter of the preselection sub-assembly (19) or of the 20 dB push button is defective!
Is there a voltage of about 6.9 mV at connection point (19) 31 ?
Is there a voltage of about 11 mV at the collector of T 1901?
Preselection (29) is defective!
Frequency identification (23) is defective!
Open up level regulating circuit at connection point (19) 30; connect R 1943 to chassis, at connection point (19) 31 attach 100 Ω against chassis. With push button [33] (S 1901) depressed, decrease test voltage at RMS-4 to -34 dBm. Are the voltages at connection point (19) 36 (about 2.2 mV) and at collector of T 1902 (about 7 mV) correct?
Preselection (19) is defective!
Is there a $\Delta U/U_o$ result at connection point (21) 120 of the rectifier (21), plate [697-BN] ?
Cross-fader (22) is defective!
Rectifier (21) is defective!
Is there a voltage of about 55 mV at connection point (20) 142 of the selection (20), plate [697-BO] or [697-BU] ?
Selection (20) is defective!
Is there a voltage of about 1 V at the collector of T 2106 of the rectifier sub-assembly (21), plate [697-BN] ?
Rectifier (21) is defective.
See next page for continuation of trouble-shooting plan!


YES
Correction device T 1904, T 1905 in the preselection sub-assembly (19) is defective!
Does the regulating voltage at connection point (21) 122 change as the input level is altered?
Rectifier (21) is defective!
Is there U_x voltage 5 V_{pp} at connection point (21) 123?
U_x generation (16) is defective!
Continuation of trouble shooting plan "No $\Delta U/U_o$ test result"
Does the DC voltage at connection point (21) 120 change as the input level is altered?
Rectifier (21) is defective!
NO

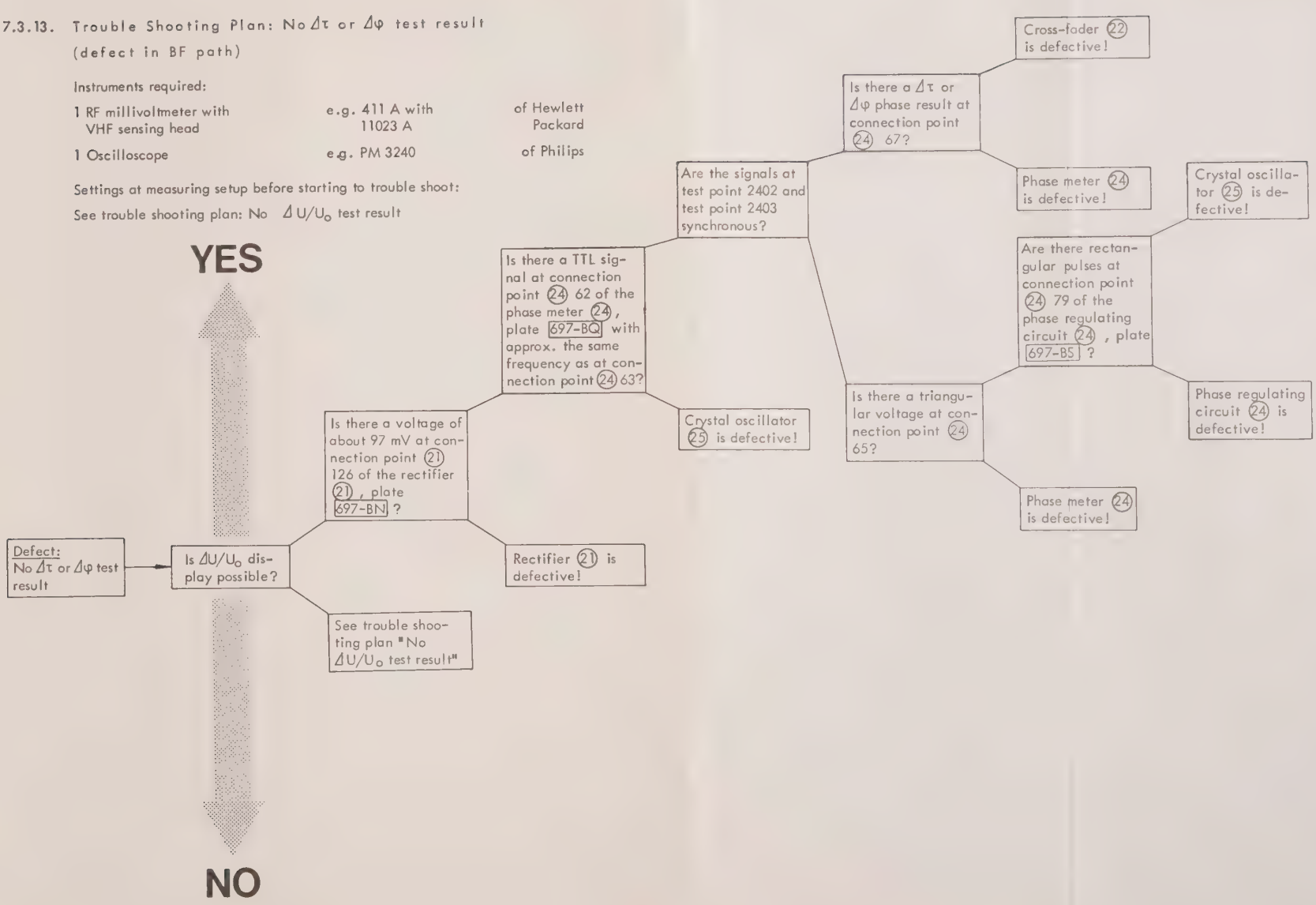
7.3.13. Trouble Shooting Plan: No $\Delta\tau$ or $\Delta\varphi$ test result (defect in BF path)

Instruments required:

1 RF millivoltmeter with VHF sensing head	e.g. 411 A with 11023 A	of Hewlett Packard
1 Oscilloscope	e.g. PM 3240	of Philips

Settings at measuring setup before starting to trouble shoot:

See trouble shooting plan: No $\Delta U/U_o$ test result


YES
NO
Defect: No Δτ or Δφ test result
Is ΔU/U₀ display possible?
See trouble shooting plan "No ΔU/U₀ test result"
Is there a voltage of about 97 mV at connection point (21) 126 of the rectifier (21), plate 697-BN ?
Rectifier (21) is defective!
Is there a TTL signal at connection point (24) 62 of the phase meter (24), plate 697-BQ with approx. the same frequency as at connection point (24) 63?
Crystal oscillator (25) is defective!
Are the signals at test point 2402 and test point 2403 synchronous?
Is there a triangular voltage at connection point (24) 65?
Phase meter (24) is defective!
Are there rectangular pulses at connection point (24) 79 of the phase regulating circuit (24), plate 697-BS ?
Phase regulating circuit (24) is defective!
Crystal oscillator (25) is defective!
Is there a Δτ or Δφ phase result at connection point (24) 67?
Phase meter (24) is defective!
Cross-fader (22) is defective!

7.3.14. Trouble Shooting Plan: Visual Display

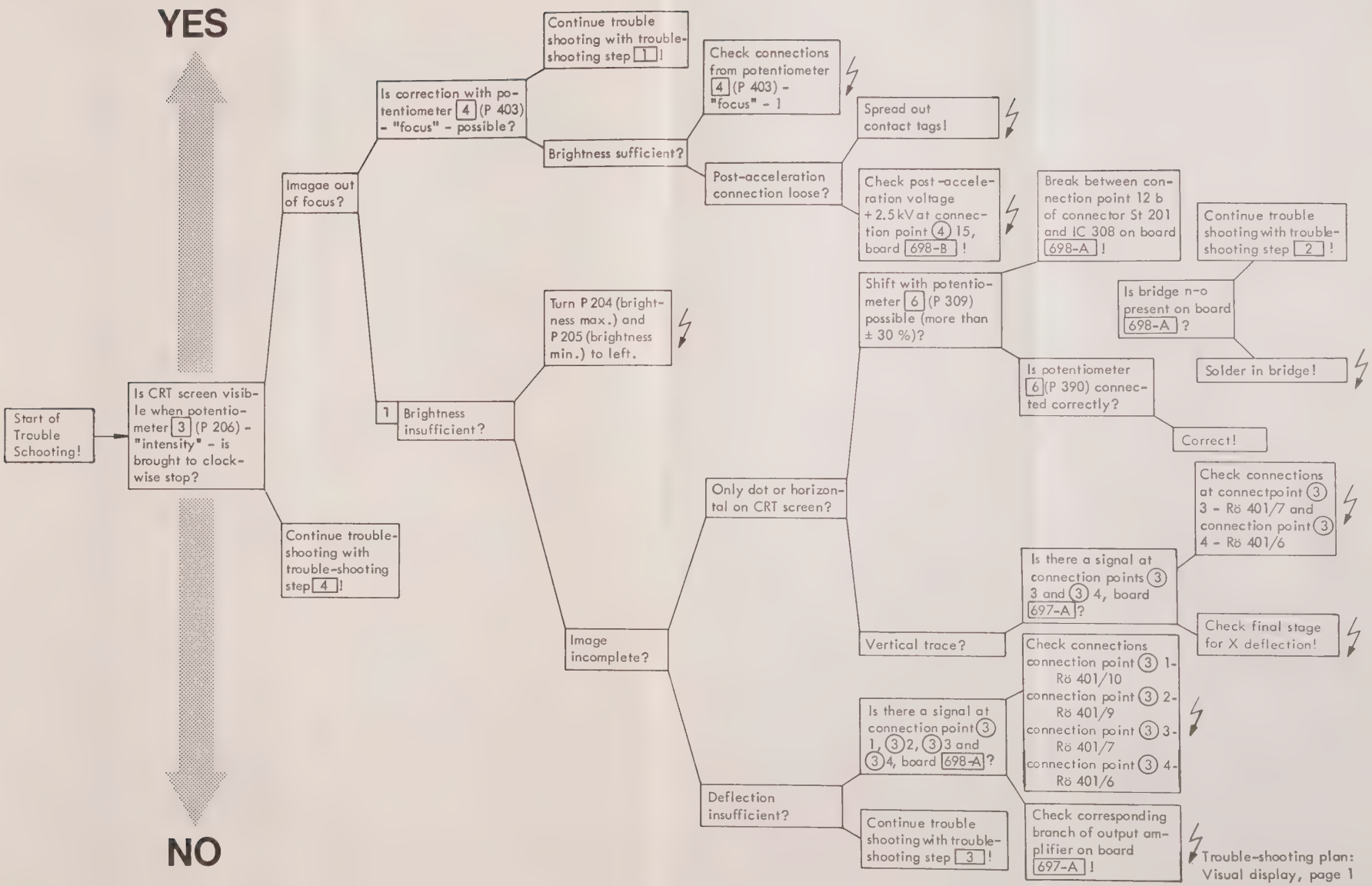
Instruments required:

1 Oscilloscope	e.g. PM 3240	of Philips
1 Digital voltmeter	e.g. 8000 A	of Fluke
1 High-voltage sensing head	e.g. 80 K-40	of Fluke

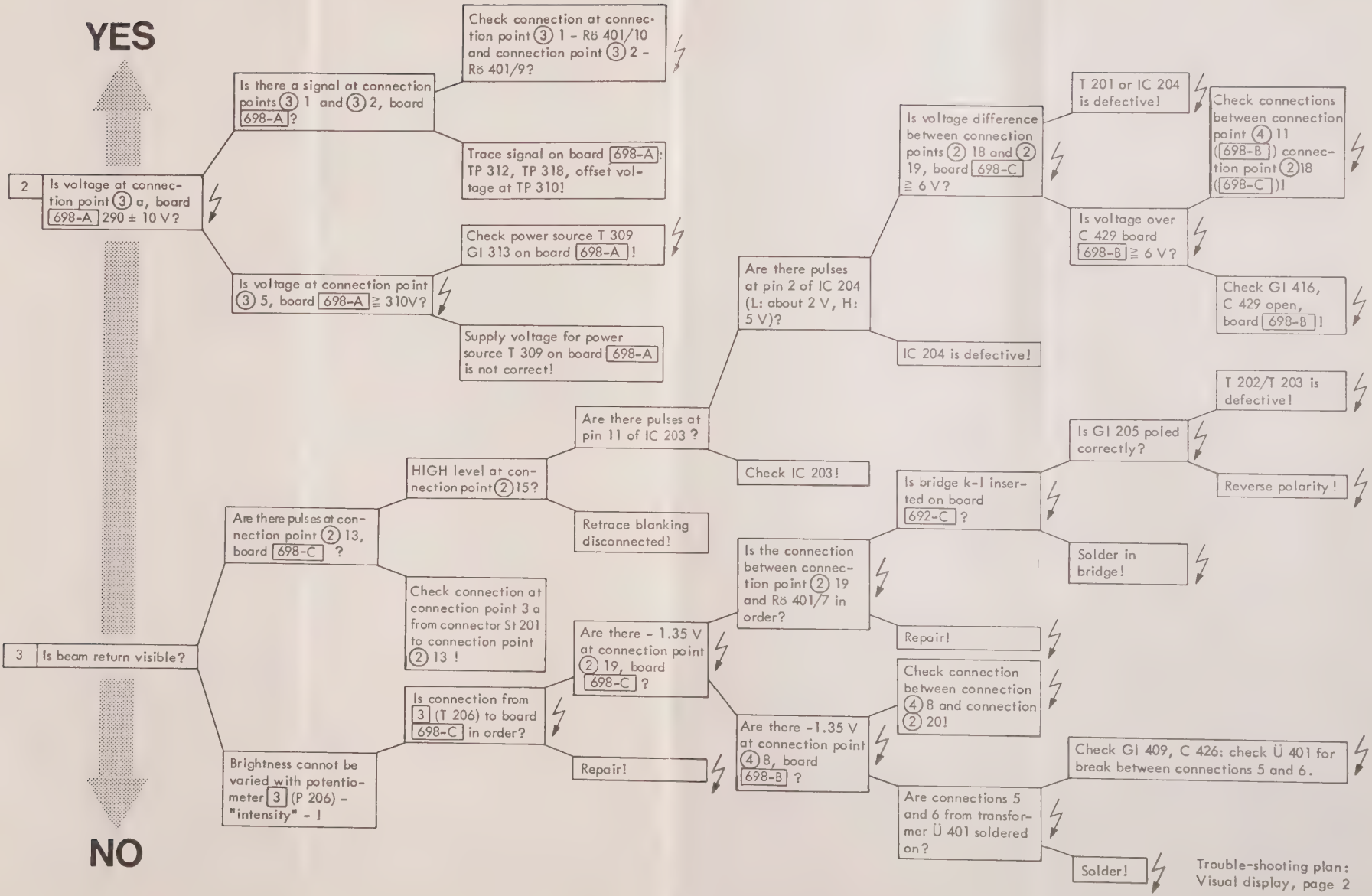
Advice for Trouble Shooting:

There are dangerous voltages on the circuit boards of the visual display. Therefore use only insul tools! Observe safety procautions! Measurements at the high voltages, especially on board 698-C may only be made with a high-voltage sensing head or via a series resistor $\geqq$ 10 KΩ.

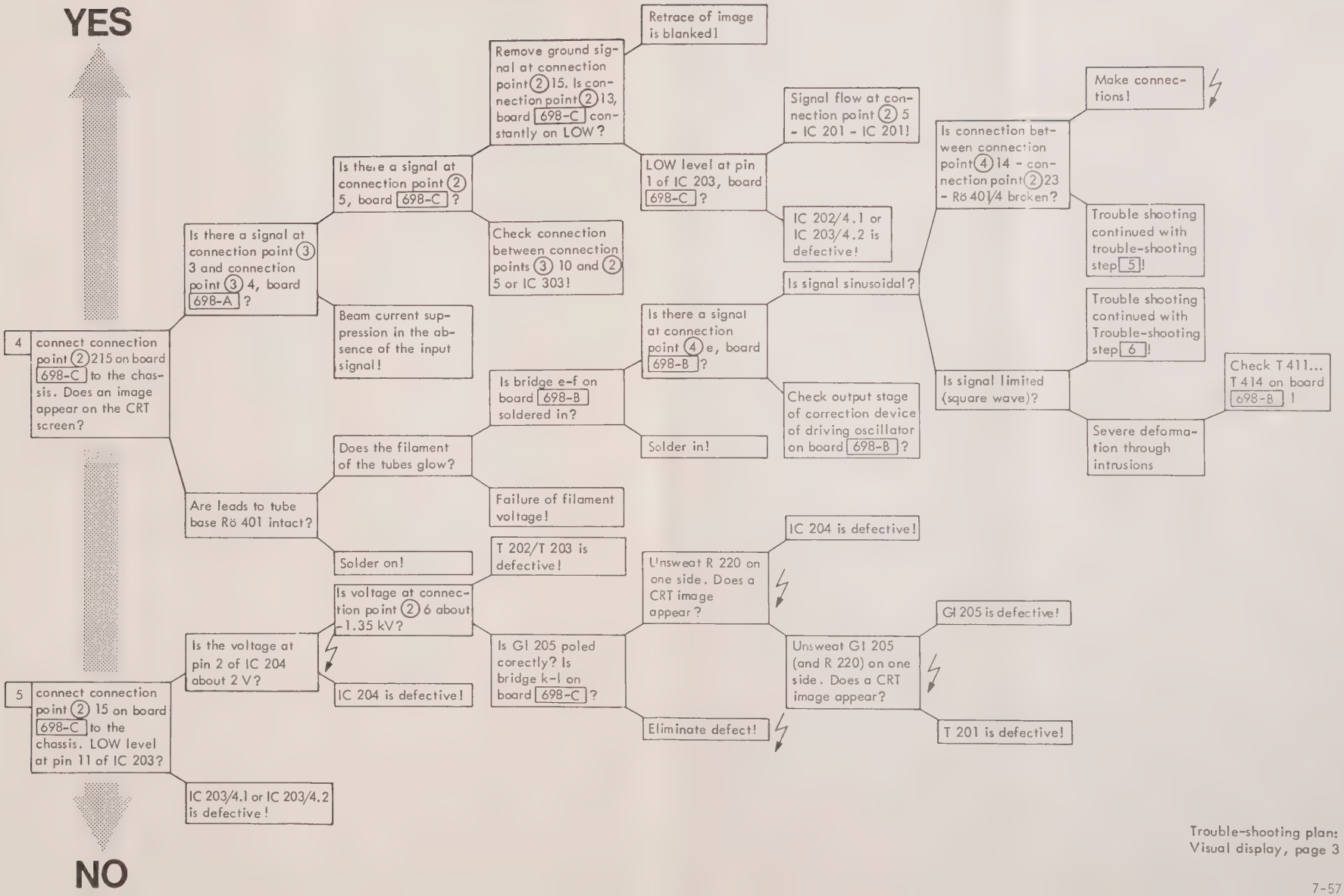
The trouble-shooting plan for the visual display consists of four pages, which are logically connected with one another. Trouble shooting should therefore always be started on page 1. Transition from one page to the next is accomplished by reference to the numbers with which the trouble-shooting steps are provided. Mistakes are therefore prevented.


YES
NO
Start of Trouble Schooting!
Is CRT screen visible when potentiometer 3 (P 206) - "intensity" - is brought to clockwise stop?
Continue trouble-shooting with trouble-shooting step 4 !
Imagae out of focus?
Is correction with potentiometer 4 (P 403) - "focus" - possible?
Continue trouble shooting with trouble-shooting step 1 !
1
Brightness insufficient?
Turn P 204 (brightness max.) and P 205 (brightness min.) to left.
Image incomplete?
Brightness sufficient?
Check connections from potentiometer 4 (P 403) - "focus" - 1
Post-acceleration connection loose?
Spread out contact tags!
Check post-acceleration voltage +2.5 kV at connection point (4) 15, board 698-B !
Break between connection point 12 b of connector St 201 and IC 308 on board 698-A !
Only dot or horizontal on CRT screen?
Shift with potentiometer 6 (P 309) possible (more than ± 30 %)?
Continue trouble shooting with trouble-shooting step 2 !
Is bridge n-o present on board 698-A ?
Solder in bridge!
Is potentiometer 6 (P 390) connected correctly?
Correct!
Vertical trace?
Is there a signal at connection points (3) 3 and (3) 4, board 697-A ?
Check connections at connectpoint (3) 3 - Rö 401/7 and connection point (3) 4 - Rö 401/6
Check final stage for X deflection!
Deflection insufficient?
Is there a signal at connection point (3) 1, (3) 2, (3) 3 and (3) 4, board 698-A ?
Check connections connection point (3) 1 - Rö 401/10 connection point (3) 2 - Rö 401/9 connection point (3) 3 - Rö 401/7 connection point (3) 4 - Rö 401/6
Continue trouble shooting with trouble-shooting step 3 !
Check corresponding branch of output amplifier on board 697-A !

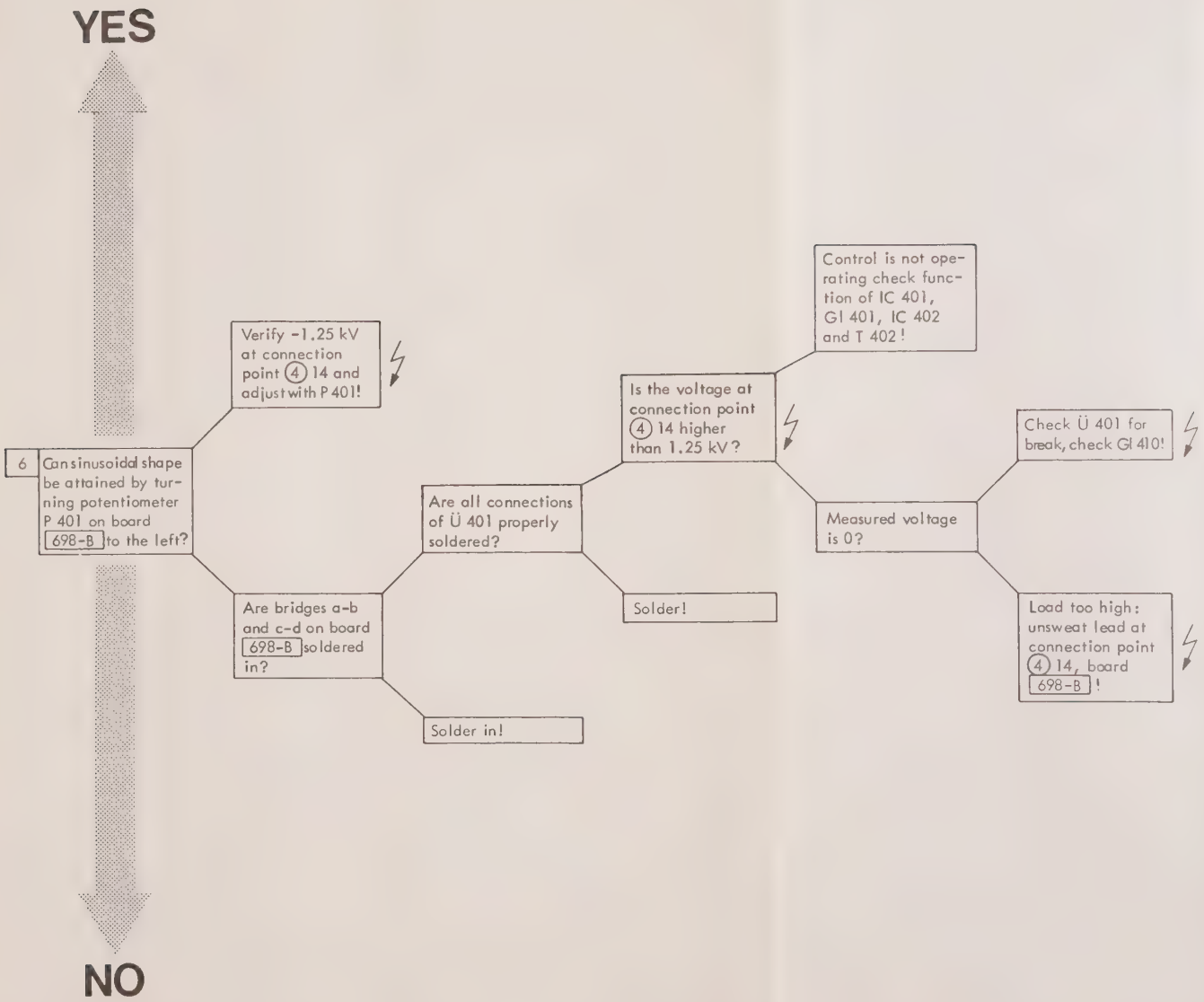
Trouble-shooting plan: Visual display, page 1


YES
2 Is voltage at connection point (3) a, board 698-A 290 ± 10 V?
Is there a signal at connection points (3) 1 and (3) 2, board 698-A?
Check connection at connection point (3) 1 - Rö 401/10 and connection point (3) 2 - Rö 401/9?
Trace signal on board 698-A: TP 312, TP 318, offset voltage at TP 310!
Check power source T 309 GI 313 on board 698-A !
Is voltage at connection point (3) 5, board 698-A ≧ 310V?
Supply voltage for power source T 309 on board 698-A is not correct!
3 Is beam return visible?
Are there pulses at connection point (2) 13, board 698-C ?
HIGH level at connection point (2) 15?
Retrace blanking disconnected!
Check connection at connection point 3 a from connector St 201 to connection point (2) 13 !
Brightness cannot be varied with potentiometer 3 (P 206) - "intensity" - !
Is connection from 3 (T 206) to board 698-C in order?
Repair!
Are there pulses at pin 11 of IC 203 ?
Check IC 203!
Are there - 1.35 V at connection point (2) 19, board 698-C ?
Are there -1.35 V at connection point (4) 8, board 698-B ?
Are there pulses at pin 2 of IC 204 (L: about 2 V, H: 5 V)?
IC 204 is defective!
Is the connection between connection point (2) 19 and Rö 401/7 in order?
Repair!
Check connection between connection (4) 8 and connection (2) 20!
Are connections 5 and 6 from transformer Ü 401 soldered on?
Solder!
Check GI 409, C 426: check Ü 401 for break between connections 5 and 6.
Is voltage difference between connection points (2) 18 and (2) 19, board 698-C ≧ 6 V?
T 201 or IC 204 is defective!
Check connections between connection point (4) 11 (698-B) connection point (2) 18 (698-C)!
Is voltage over C 429 board 698-B ≧ 6 V?
Check GI 416, C 429 open, board 698-B !
Is bridge k-l inserted on board 692-C ?
Solder in bridge!
Is GI 205 poled correctly?
Reverse polarity !
T 202/T 203 is defective!
NO

Trouble-shooting plan: Visual display, page 2


YES
4 connect connection point (2) 215 on board 698-C to the chassis. Does an image appear on the CRT screen?
Is there a signal at connection point (3) 3 and connection point (3) 4, board 698-A ?
Beam current suppression in the absence of the input signal!
Is there a signal at connection point (2) 5, board 698-C ?
Check connection between connection points (3) 10 and (2) 5 or IC 303!
Remove ground signal at connection point (2) 15. Is connection point (2) 13, board 698-C constantly on LOW?
Retrace of image is blanked!
LOW level at pin 1 of IC 203, board 698-C ?
Signal flow at connection point (2) 5 - IC 201 - IC 201!
IC 202/4.1 or IC 203/4.2 is defective!
Are leads to tube base Rö 401 intact?
Solder on!
Does the filament of the tubes glow?
Failure of filament voltage!
Is bridge e-f on board 698-B soldered in?
Solder in!
Is there a signal at connection point (4) e, board 698-B ?
Check output stage of correction device of driving oscillator on board 698-B ?
Is signal sinusoidal?
Is connection between connection point (4) 14 - connection point (2) 23 - Rö 401/4 broken?
Make connections!
Trouble shooting continued with trouble-shooting step 5!
Is signal limited (square wave)?
Trouble shooting continued with Trouble-shooting step 6 !
Severe deformation through intrusions
Check T 411... T 414 on board 698-B !
5 connect connection point (2) 15 on board 698-C to the chassis. LOW level at pin 11 of IC 203?
IC 203/4.1 or IC 203/4.2 is defective!
Is the voltage at pin 2 of IC 204 about 2 V?
IC 204 is defective!
Is voltage at connection point (2) 6 about -1.35 kV?
T 202/T 203 is defective!
Is Gl 205 poled corectly? Is bridge k-l on board 698-C ?
Eliminate defect!
Unsweat R 220 on one side. Does a CRT image appear ?
IC 204 is defective!
Unsweat Gl 205 (and R 220) on one side. Does a CRT image appear?
Gl 205 is defective!
T 201 is defective!
NO

Trouble-shooting plan:
Visual display, page 3


YES
6
Can sinusoidal shape be attained by turning potentiometer P 401 on board 698-B to the left?
Verify -1.25 kV at connection point (4) 14 and adjust with P 401!
Are bridges a-b and c-d on board 698-B soldered in?
Solder in!
Are all connections of Ü 401 properly soldered?
Solder!
Is the voltage at connection point (4) 14 higher than 1.25 kV?
Control is not operating check function of IC 401, Gl 401, IC 402 and T 402!
Measured voltage is 0?
Check Ü 401 for break, check Gl 410!
Load too high: unsweat lead at connection point (4) 14, board 698-B!
NO

Trouble-shooting plan:
Visual display, page 4

7.3.15 DEFECTS IN THE BF LEVEL METER

Measuring instruments required:

1 Level Generator	e.g. PS-14	supplied by W&G
1 Selective Level Meter with Test Probe TK-11	e.g. SPM-14	supplied by W&G
1 digital voltmeter	e.g. 8600A	supplied by Fluke

Advice for troubleshooting:

The BF level meter is divided into two modules. The indication circuit with decoder and calibrated oscillator (34) is located behind the front panel of the lower plug-in unit. The other circuit (32) and (33) is located on a plug-in board in the upper, right-hand plug-in unit. This plug-in board [697-CJ] can be raised using the adapter board [697-AT] to make the components on the board accessible.

Recognized defects:

1. No level indication and GL 3406 or GL 3407 lights up although the applied level lies within the measuring range.
   See 7.3.15.1.
2. Level search routine does not stop
   See 7.3.15.2.
3. Regulating circuit does not function
   See 7.3.15.3.

7.3.15.1 No Level Indication

Move switch [29] (S 1601) to position "BF level, P_{BF}"
Check level in accordance with level diagram 7-1
For this, the regulating circuit must be blocked as follows:

- Move switch [42] (S 3401) to position "ΔP_{BF}"
- Disconnect strap e-f on the pc board [697-CH]
- Connect soldering lug f to +5 V (this erases memory IC 3317 and switches RF amplifier (32) to maximum gain)

7.3.15.2 Level Search Routine Does Not Stop

Possible causes:

a) Defect in the control circuit (33); if so, see 7.3.15.3.
b) Attenuators in RF amplifier (32) do not operate correctly; if so,
- block control circuit as in 7.3.15.1. and erase memory

- move switch [29] (S 1601) to position "BF level, P_{BF}"
- feed measuring level via socket [30] (Socket 1901) at f = 100 kHz
- measure level at Point (32) 40 using Test Probe and Selective Level Meter
- check function of the attenuators in accordance with Table 7-3 Permissible deviation of the output level $\leq$ 0.02 dB.

Input level at socket[30]		Relay	Atten-uator	Output level at point(32)40
- 50 dBm	-	-	-	- 10 dBm
- 30 dBm	Connect Point 33 to earth	3201	20 dB	- 10 dBm
- 40 dBm	Connect Point 34 to earth	3202	10 dB	- 10 dBm
- 48 dBm	Connect Point 35 to earth	3203	2 dB	- 10 dBm
- 46 dBm	Connect Point 36 to earth	3204	4 dB	- 10 dBm
- 44 dBm	Connect Point 37 to earth	3205	6 dB	- 10 dBm
- 42 dBm	Connect Point 38 to earth	3206	8 dB	- 10 dBm
- 49 dBm	Connect Point 32 to earth	G13201	1 dB	- 10 dBm

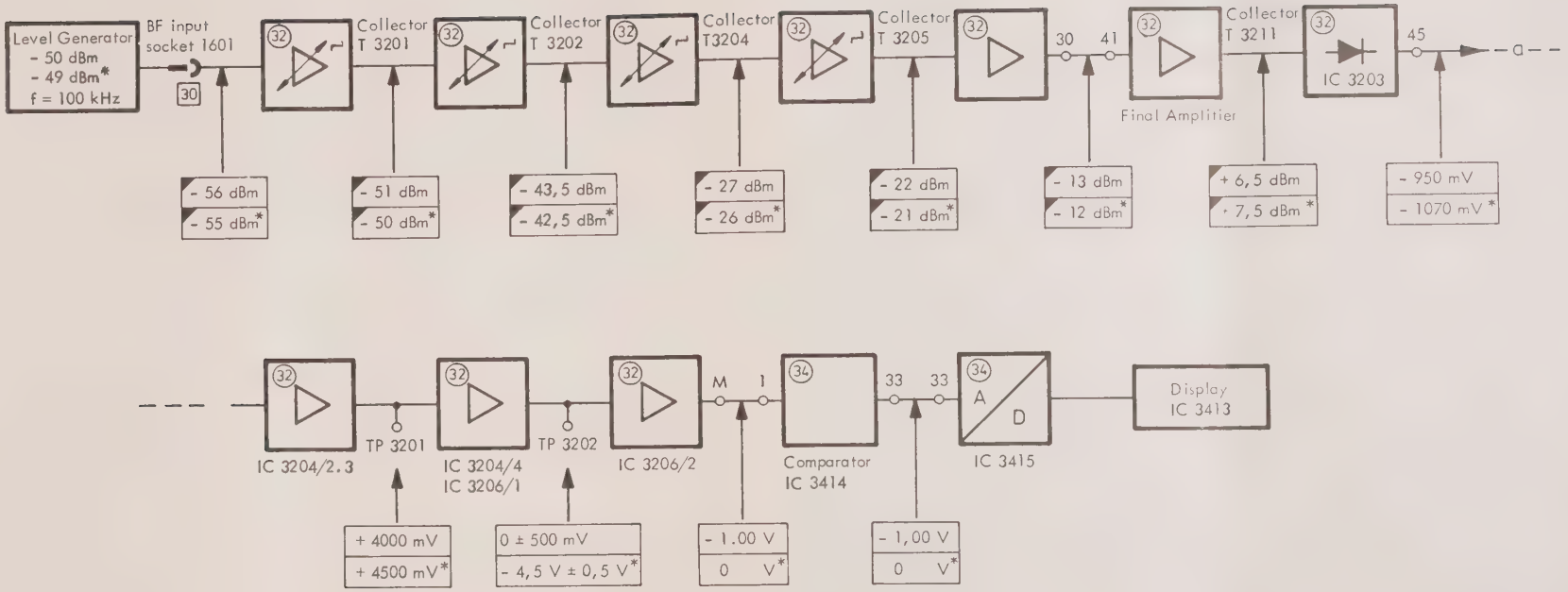
Table 7-3

7.3.15.3 Defects in the Control Unit (33)

a) Supply -50 dBm, f $\approx$ 100 kHz to Level Meter input socket [30] (socket 1901); approximately -1 V must now be present at Point (33) 49 [697-CA]. Check the logic states in accordance with Table 7-4, Column A, below.

b) Disconnect strap a-b; connect bounce-free push- button to Point b to generate single H-pulses. Increase level at input until +0.6 V is present at Point (33) 49. Connect Digital Probe TKL-515 to Point (33) 55. Generate a single pulse at Point b; an L-pulse must appear at Point 55. Recheck the logic states in accordance with Column B.

c) Generate a further single pulse at Point b; check the logic states in accordance with Column C



The stated values depend on the accuracy of the input level.

Potentiometer "Cal." [41] (P 3203) should be turned to the middle setting before commencing measurement.

Measurement using Level Meter and Test Probe, e.g. SPM-14 and TK-11 from W&G.

Measurement using digital voltmeter 4 1/2 digit, e.g. Fluke 8600 A

Fig. 7-9 Level diagram BF level meter

d) As 4.3., check in accordance with Column D

e) As 4.3., check in accordance with Column E

f) Reduce input level until -1 V is present at Point 49. Generate at least 4 clock pulses at Point b (erasing of the shift register IC 3309).
Lower input level again until -2.6 V is present at Point 49. Generate 4 single pulses at Point b.
Check the logic states in accordance with Column F

g) Raise input level again so that +0.6 V is present at Point 49. Generate 2 clock pulses at Point b. Check the logic states in accordance with Column G.

h) Lower input level until -2.6 V is present at Point 49. Generate one single pulse at Point b. Check the logic states in accordance with Column H.

i) As 4.8., check in accordance with Column I

k) Increase input level until -2.0 V is present at Point 49. Generate one single pulse at Point b. Check the logic states in accordance with Column K.

Table of logic states

Meas.point	A	B	C	D	E	F	G	H	I	K
Strap e-f	L	H	H	H	H	L	H	H	H	H
Strap g-h	L	L	H	H	H	L	H	H	H	H
Strap i-k	L	L	L	H	H	L	L	H	H	H
Strap l-m	H	H	H	H	L	H	H	H	L	L
Point 52	L	L	L	H	L	L	L	H	L	H
Point 53	L	L	L	H	H	L	L	H	H	L
Point 54	H	H	H	H	H	L	H	L	L	L
Point 56	L	H	H	H	H	L	H	L	L	L
IC 3318/5	L	L	L	L	L	L	L	L	L	H
IC 3318/3	L	L	L	H	H	L	L	H	H	H
IC 3318/14	H	H	H	L	L	L	H	H	H	H
IC 3318/12	L	L	L	H	L	L	L	L	H	H
Point H	L	L	L	L	L	L	L	L	L	H
Point J	L	L	L	L	H	L	L	L	L	H
Point K	L	L	L	L	L	L	L	L	L	H
Point F	L	L	L	L	L	L	L	L	H	L
Point 5	L	L	L	H	H	L	L	H	L	L
Point E	L	L	H	H	H	L	H	L	L	L

Table 7-4

7.4. Dismantling Operations

Advice: The instrument is to be switched off and unplugged during dismantling operations!

7.4.1. Disassembly of the Plug-In Units

The disassembly of the three plug-in units (visual display, upper right and lower plug-in parts) from the completely assembled RME-4 proceeds as follows:

- Place instrument in use position and remove lid; for this purpose, remove 6 hexagonal socket-head bolts with the wrench supplied (compare advice in Section 7.1.)
- Place instrument on right side wall and pull out plug-in part, consisting of the visual display and the upper right plug-in part which are mechanically connected with one another, and place next to housing of instrument.
- Undo the 7-pole plug and socket connector Bu/St 102 (voltage supply for the visual display) at the power supply.

Note: This plug and socket connector is mechanically latched; to separate, press the two oppsitely located latching devices in order to release the upper plug section and to enable its withdrawal.
Caution! The contact pins of the plug might have a voltage remaining for a short time after the instrument has been switched off.

- Unlock the holders at the 2 x 18-pole plug connector (697-7002.012) at the underside of the pull-out plug-in part and pull out plug connector from the socket connector.
- Loosen the subminax connection at plug connector St 1704 at the lower plug-in unit
- Plug-in part unit is now also disconnected electrically.

In order to separate the visual display mechanically from the upper right plug-in part, the procedure below is followed:

- Bring plug-in part unit into use position.
- Loosen front and rear bracket with the wrench supplied until the two plug-in parts can be pulled apart.
- Undo two 22-pole plug and socket connector Bu 104/St 201.

The disassembly of the lower plug-in unit proceeds as follows:

- After disassembling the upper plug-in part, bring plug-in part again into use position.
- Loosen the three 8-pole plug and socket connector St/Bu 1, St/Bu2 and St/Bu 101.
- Lift the lower plug-in part out of the instrument.

Advice: Before lifting out the lower plug-in part, the spare fuses are to be taken out of the housing recess on the back panel of the instrument. Because of the sub-assembly with power supply line filter and mains voltage selector, it is not possible to disassemble the lower plug-in part by removing the sheet-metal cover at the base of the instrument.

If trouble shooting immediately precedes the repair of the instrument, it is possible to start from a state of disassembly and a position of the instrument corresponding to Section 7.1. and Figure 7-1. The upper plug-in parts are practically free and it is only necessary to undo the electrical connections.

After disconnecting from the power supply, the lower plug-in part

is detached from the right side wall by pushing sideways in the guide grooves. The above advice is to be observed.

7.4.2. Disassembly of the Power Supply

The power supply forms a unit with the right side wall. If the power supply is to be dismantled from a completely assembled instrument, the procedure below is to be followed:

- Place the instrument on the left side wall.
- Remove lid and bottom.
- Undo cable connection between power supply and plug-in units (plug and socket connectors St/Bu 1, St/Bu 2, St/Bu 101, St/Bu 102)
- Now shift right side wall in guide grooves until it is no longer prevented from being lifted off by the sub-assembly with mains voltage selector.

7.4.3. Removing and Attaching Control Knobs

For the purpose of eventually reattaching them, the control knobs are to be brought into a defined position before their removal. The removal proceeds as follows:

- Lift off cover of control knob with a knife.
- Detach clamping cone with a socket wrench or a screw driver, depending on the type of control knobs.
- Pull off control knob from axle; if the clamping cone does not become loose automatically, knock lightly against control knob.

7.4.4. Disassembly of Printed Circuits

For reasons of shielding, the printed circuits are housed in enclosed metallized plastic tubs. In order to disassemble a

printed circuit, the lid must first of all be lifted from the tub by the plastic loop provided for this purpose.

When the connection leads have been unsweated or all plug and socket connectors detached, all Phillips screws, which are used for attaching the board, are to be removed. The printed circuit can than be lifted out of the tub - the majority of boards are provided with a special card puller for this purpose.

7.4.5. Disassembly of the Demodulator Component

- Disassemble lower plug-in unit from the instrument (compare Section 7.4.1.) and bring into use position with back panel in view.
- Remove printed cover plate from back panel (5 oval - head screws)
- Remove 2 Phillips countersunk screws (M3) in the lower right hand section of the back panel.
- Remove 4 cheese-head screws (M2,6) in the middle of the back panel at the right.
- Remove 6 Phillips countersunk screws (M5) along the whole width of the middle of the back panel.
- Carefully lift back panel from plug-in unit until the demodulator component can be pulled out (compare Figure 7-4).

7.4.6. Disassembly of Attenuator Set

- Disassemble lower plug-in unit (see Section 7.4.1.) and place in use position with front plate in view.
- Unsweat gray/red lead in input amplifier (7) sub-assembly on board 697-V.. from soldering terminal (applies only for Series B)

- Undo HF connection between attenuator set and input amplifier (7) sub-assembly at St 702.
- Remove control knobs from front plate (see Section 7.4.3.)
- Remove any reducers from the universal sockets (with wrench W1 for Versacon (R) lock nuts)
- Remove printed cover plate (5 oval-head screws).
- Place plug-in unit upright on the power-cable bracket at the rear (with underside of plug-in in view).
- Detach 3 clamps of cable-harness attachment (starting from left).
- Detach hinged support of the 2 hinged chassis at the lower edge of the front plate (a total of 6 Phillips countersunk screws M3)
- Remove attachment loops for an HF lead and a cable harness from the housing brace of the attenuator set.
- Detach socket [27] (Bu 1) from the front plate, from Series C onwards also socket [28] (Bu 1701).
- Detach attenuator set from the front plate (4 Phillips countersunk screws M5)
- Detach front plate from the struts of the plug-in part (3 Phillips countersunk screws M5)
- Carefully lift front plate from plug-in part until the attenuator set can be lifted out between the front plate and the plug-in part.

7.4.7. Detaching the Hinged Chassis

A portion of the ciruits were accommodated on the hinged chassis in order to have easier access to the circuit boards lying deeper in the instrument. There are 2 hinged chassis on the underside of the lower plug-in part. In order to swing them out, 2 Phillips oval-head screws have to be removed from each. In the case of the smaller hinged chassis, the screw driver guide tube for adjusting

potentiometer 52 (P 1605) must previously be removed with the help of a hexagonal pin wrench (SW 1,2) and pulled out of the instrument until it no longer interferes with the swinging out of the chassis (compare Figures 7-3 and 7-4). Because of a mechanical change, this process is no longer required from Series D onwards. The third hinged chassis is located on the right side of the visual display. After removing 4 Phillips oval-head screws, it can be swung out in the disassembled state of the visual display (see Figure 7-7).

7.4.8. Disassembly of the Plug-In Cards

In the upper right plug-in part, several plug-in cards are accommodated which are secured with a restraining strut in order to prevent their falling out unintentionally. After removing this restraining strut, the plug-in cards can be pulled out of the plug-in. The arrangement of the plug-in cards is printed on the restraining strut in order to prevent a mix up during the assembly.

7.4.9. SOLDERING AND UNSOLDERING OF CHIP COMPONENTS

Necessary tool:

Soldering iron with temperature control and forked tip, e.g. Weller-Magnatstat (50 to 80 W) with Group 5 soldering tip (up to 260°C) or Group 6 (up to 310 °C) or, as appropriate, adjustable soldering iron Zeva G5T (65 W), setting: 280°C.

Tin type C3 (Ø 1 mm) with 1.5 % rosin-core should be used for soldering.

When soldering and unsoldering, the maximum permissible temperature at the soldering point is 240°C. This temperature will not be exceeded if the soldering time is kept as short as possible (max. 3 s).

When soldering, the soldering position on the component side of the pc board should be pre-tinned. The component is then placed with the connection surfaces on the soldering position. Both soldering points on the printed conductors should then be heated simultaneously using the forked soldering tip; when doing this, the component must not be touched with the soldering tip. If necessary, the component should be held in position during soldering with a wooden stick. If two chips are to be soldered which are located next to one another, a short period should be allowed for cooling off after the first chip has been soldered. Chip capacitors may only be held using metal pincers on the contact surfaces.

8. CHECKING IMPORTANT TECHNICAL DATA

In the following, procedures are described which permit the important characteristic values of the instrument to be checked. Where possible, conventional means of measuring are proposed. Unless limited further by a recommendation, all tests should be carried out within the nominal use ranges for temperature and mains voltage.

If a warming-up period is specified for the technical data, the tests should not be commenced until after this time.

Checking the important data is intended to establish whether the data measured lies within the guaranteed area limits. Checking is successful only if the inherent errors of the measuring set-up are neglegibly small.

Normally, the following rules apply:

If the guaranted limits of error for the component to be tested are given as ±e and if the error of the measuring set-up used is ±m,

the guaranted limits of error
are certain to be exceeded
if the limits ± (e + m) are exceeded:

the guaranted limits of error
are certain to be observed
if the limits ± (e - m) are not exceeded.

The value of e is given for each set of measuring instructions. The value of m depends on the measuring instrument used and generally therefore must be determined from case to case. The set of measuring instructions is compatible with the value of m, only if the means employed for measuring permit no variation or if no other conditions must be taken into consideration.

In any systematic checking of the data, the sequence of procedures given here should be followed.

A readjustment of the component should be carried out only when it has been established that the limit ± (e + m) has been exceeded.

The most important technical data of the RME-4 are checked with the RMS-4 and RME-4 in back-to-back connection.

With this procedure, only the overall defects of the combination of instruments RMS-4/RME-4 can be determined. It will not be possible in every case to determine the errors specific to one instrument. Accordingly, various defect limits are defined for the back-to-back operation already in Chapter 1.

> In the case of back-to-back measurements, care must be taken that the instruments which belong together, namely RMS-4 and RME-4, are used for the measurement. Information in respect to this may be found on the back panel of the instrument.

If the error limits are noted to deviate from the given values, it is necessary to establish, by checking the data of the RMS-4 (see chapter 8 of the service manual of the RMS-4), at which of the two instruments re-adjustment is required. Re-adjustment of the RME-4 is described in Chapter 9 of this service manual.

8.1. Distortion Measurements $\Delta\tau$, $\Delta\varphi$ and $\Delta U/U_o$

8.1.1. Accuracy of Indication in the Case of Distortion Measurements

Instruments required:

1 Level Measuring Setup	e.g. PSM-14 of W&G
1 2-way Switch	e.g. REV-56 of W&G

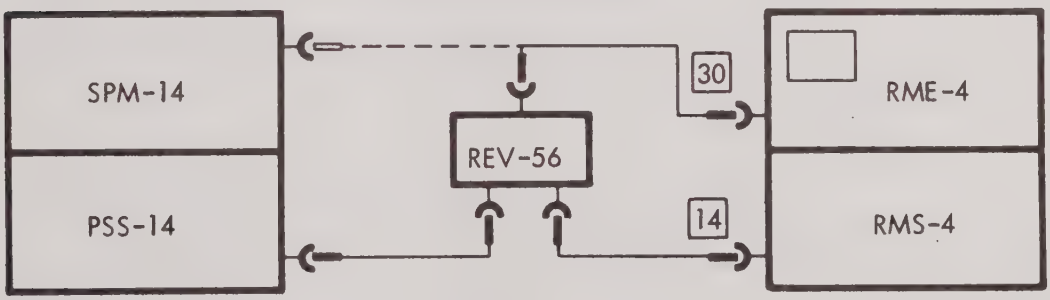


Fig. 8-1 Measuring setup for Section 8.1.1.

Settings of the instrument:

RMS-4:	[15]	(S 1601):	Both keys depressed (≙40 dB)
	[16]	(S 1501):	Fully anticlockwise
	[17]	(P 1305):	5 V (fully clockwise)

	[7]	(S 1301):	Off
	[20]	(S 1302):	70 Hz
RME-4:	[29]	(S 1601):	Input BB (Distortion)
	[33]	(S 1901):	Depressed (-30 to -10 dBm)
	[34]	(S 1602):	U_x from BB
	[2]	(S 2201):	⁓ (calibration lines on)
	[9]	(S 2203):	Key "$\Delta\varphi$, $\Delta\tau$" depressed
	[23]	(S 2204):	Key "$\Delta U/U_o$" depressed
	[11]	(S 601) :	6 kHz/0 MHz

PSS-14: Level setting 0 dBm

SPM-14: Bandwidth 360 Hz, measuring range -10 dBm, expanded indication

Heating-up period for the measuring setup: ca. 0.5 hours!

Preparatory settings (required before each change of test frequency):

- Initially, connect output lead of the REV-56 with the level meter
- Adjust level setup to the measuring frequency f_M selected at the RMS-4 and read off level indication at the level meter (ca. -10 dBm)
- Sweep level sender and, for this purpose, adjust the measuring voltage U_M at the RMS-4 with potentiometer [16] (P 1501) so that the same indication results at the level meter as in the step before (for this purpose, release keys [15]). At the same time, the level meter is to be tuned exactly to the measuring frequency.

(= level maximum). Now the magnitudes of the test and of auxiliaries voltages are the same for the measuring frequency chosen.

Note: With BB Level Meter equipped instruments, the test voltage and the auxiliary voltage can be set to equal values by use of this integral level meter. For this purpose, switch [29] is switched to the "BB Level" position.

Measurement:

- Connect REV-56 with the BB input [30] (Bu 1901) of the RME-4
- Adjust auxiliary voltage at the level sender according to Table 8-1
- Adjust the frequency $f_M + 2\ f_A$ at the level measuring setup. When the adjustment has been made correctly, a sinusoidal signal with a whole period is seen on the CRT screen. If the frequency tuning is changed a little, a series of slightly displaced waves appear. The envelope curves of the waves formed resembles a circle (see Figure 8-2).

Stellung der Meßbereichsschalter		Sollwerte der Hilfsspannungen [dBm]					
		für $\Delta\tau$				für $\Delta\varphi$	für $\Delta U/U_0$
[10] $\Delta\tau$ [ns] (Multiplikator GI 1501 bis 1503 unberücksichtigt)	[10] $\Delta\varphi$ [% rad] [17] U/U_0 [%]	bei f_M= 83.3 kHz	bei f_M = 92.592 kHz	bei f_M = 250 und 500 kHz	bei f_M = 277.$\overline{7}$ und 555.$\overline{5}$ kHz	bei f > 1 MHz	bei allen f_M
100		-17.73	-16.81	-22.16	-21.25		
	50					-18.08	-18.19
40		-25.67	-24.75	-30.10	-29.19		
	20					-26.02	-26.04
20		-31.69	-30.77	-36.12	-35.21		
	10					-32.04	-32.05
10		-37.71	-36.79	-42.14	-41.23		
	5					-38.06	-38.06
4		-45.67	-44.75	-50.10	-49.19		
	2					-46.02	-46.02
2		-51.69	-50.77	-56.14	-55.21		
	1					-52.04	-52.04
1		-57.71	-56.79	-62.14	-61.23		
	0,5					-58.06	-58.06

Table 8-1

Key for Table 8-1:

Stellung der Messbereichs-schalter	=	Setting of the measuring range switches
Multiplikator G1 1501 bis 1503 unberücksichtigt	=	Multiplier G1 1501 to 1503 disregarded
Sollwerte der Hilfsspannungen (dBm)	=	Nominal values of the auxilia voltages (dBm)
für	=	for
bei	=	with
und	=	and
bei allen	=	with all

- The highest and lowest points of this circle should just touch the calibrating lines. In order to achieve this, the auxiliary voltage at the level sender as well as the zero position on the CRT screen should be changed with potentiometer [22] (P 2202) at "$\Delta U/U_0$" or [8] (P 2201) at "$\Delta\varphi$, $\Delta\tau$".

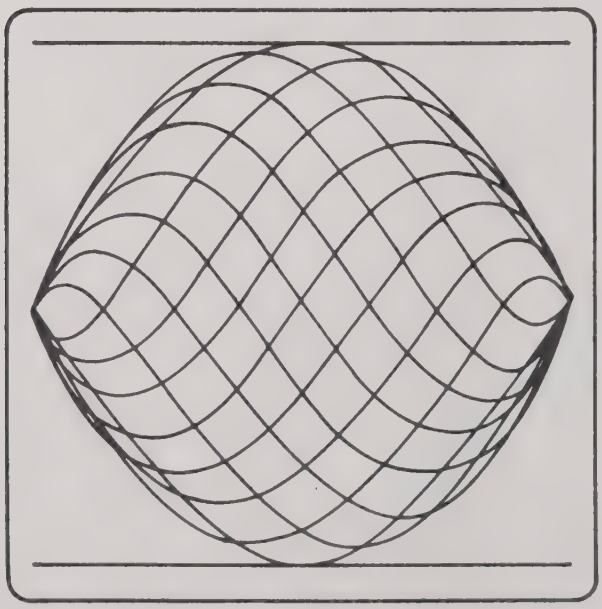


Fig. 8-2

Key for Figure 8-2;

Eichlinie = Calibrating line

- After adjustment has been made, read off level value at the level center. Determine deviation from nominal value and compare with the error limits (e).

  Error limits (e): +0.83 dB, -0.92 dB } (corresponds to the specifications of the RME-4: ±10%)

This measurement can be repeated for each setting of the measuring range switch [10] (S 2205) or [24] (S 2202) and for each measuring frequency ([19] (S 1501) at the RMS-4). If measuring ranges $\leqq$ 10% at $f_M > 1$ MHz are selected, $\Delta\varphi$ and $\Delta U/U_0$ can be checked together, because the nominal values of both quantities are the same here. For the smallest measuring ranges, the attempt should be made to average, since the intrinsic noise is superimposed on the picture here. (If a sweep frequency $f_A < 40$ Hz is built in, a further possibility exists of selecting the lower deflecting frequency [20] (S 1302) at the RMS-4 and the band width [11] (S 601) of 0.3 kHz at the RME-4.)

8.1.2. Intrinsic Distortions

Measuring setup: Back-to-back measurement RMS-4 - RME-4
Connection between P_1 - output [1] (Bu 1)
and P_1 - input [27] (Bu 1)

Advice: The back-to-back connection is to be established with the short 75 Ω cable supplied

Settings of the instrument:

RMS-4:	[2]	(P 1201):	0 dB
	[13]	(EL 601):	0 dBm
	[4]	(S 803):	70/140 MHz
	[6]	(P 1303):	±12 MHz
	[7]	(S 1301):	On
	[8]	(S 902):	Sweep
	[9]	(S 903):	70 MHz
	[16]	(P 1501):	500 kHz (right stop)
	[17]	(P 1305):	12 MHz (right stop)
	[18]	(S 801):	2 $\hat{\Delta}$F
	[20]	(S 1302):	70 Hz
RME-4:	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[33]	(S 1901):	Pressed
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	70 MHz
	[9]	(S 2203):	Pushbutton "$\Delta\varphi$, $\Delta\tau$" pressed
	[10]	(S 2205):	1 ns or 0.5% rad
	[23]	(S 2204):	Pusbutton "$\Delta U/U_o$" pressed
	[24]	(S 2202):	0.5%
	[11]	(S 601) :	6 kHz / 0 MHz

- Adjust display unit so that the results $\Delta\tau$ or $\Delta\varphi$ and $\Delta U/U_o$ are visible
- Dial through the selection of frequencies of switch [19] (S 1501) at the RMS-4 and read off the corresponding distortion values.

Compare values with the first line of Table 8-2.

- Increase sweep range [6] (P 1303) and sweepwidth [17] (P 1305) to ± 25 NHz and repeat the measurement. Compare the values with line 2 of Table 8-2.
- Switch IF [9] (S 903) and [37] (S 1402) to 140 MHz, set sweep range [6] (P 1303) and sweepwidth [17] (P 1305) to ± 18 MHz. Control intrinsic distortions for each measuring frequency. The error limits in line 3 of Table 8-2 now apply.
- Extend sweep range [6] (P 1303) and sweepwidth [17] (P 1305) to ± 30 MHz and repeat the measuring. Compare values with line 4 of Table 8-2.

ZF	Abtast-bereich	Fehlergrenzen (e) bei $f_M \leqq 1$ MHz		Fehlergrenzen (e) bei $f_M > 1$ MHz	
		$\Delta\tau$	$\Delta U/U_o$	$\Delta\varphi$	$\Delta U/U_o$
70 MHz	±12 MHz	0.4 ns	0.1 %	0.5 % rad	0.2 %
	±25 MHz	1 ns	0.3 %	1 % rad	0.4 %
140 MHz	±18 MHz	0.3 ns	0.15 %	0.5 % rad	0.2 %
	±30 MHz	0.8 ns	0.3 %	1 % rad	0.4 %

Table 8-2

Key for Table 8-2:

ZF	=	IF
Abtastbereich	=	Sweep range
Fehlergrenzen (e) bei $f_M \leqq 1$ MHz	=	Error limits (e) for $f_M \leqq 1$ MHz
Fehlergrenzen (e) bei $f_M > 1$ MHz	=	Error limits (e) for $f_M > 1$ MHz

8.2. Intrinsic Noise

8.2.1. Intrinsic Noise in the IF Plane

Measuring setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_1-output [1] (Bu 1) and P_1-input [27] (Bu 1)

Advice: The back-to-back connection is to be established with the short 75 Ω cable supplied

Settings of the instruments:

RMS-4	[2]	(P 1201):	0 dB
	[13]	(EL 601):	0 dBm
	[4]	(S 803):	70/140 MHz
	[7]	(S 1301):	Off
	[8]	(S 902):	Sweep
	[9]	(S 903):	140 MHz
	[16]	(P 1501):	200 kHz
	[17]	(P 1305):	2 MHz
	[18]	(S 801):	Off
	[20]	(S 1302):	70 Hz
RME-4	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[33]	(S 1901):	Not pressed
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	140 MHz
	[9]	(S 2203):	Pushbutton "Δφ, Δτ" pressed
	[10]	(S 2205):	1 ns or 0.5% rad

RME-4 cont. [23] (S 2204): Pushbutton "$\Delta U/U_o$" pressed

[24] (S 2202): 0.5%

[11] (S 601) : 6 kHz / 0 MHz

- Adjust display unit so that the results $\Delta\tau$ or $\Delta\varphi$ and $\Delta U/U_o$ are visible
- Dial through measuring frequency selection of switch [19] (S 1501) at the RMS-4 for $f_M < 1$ MHz and read off the width of the noisy result indication; compare the results with Table 8-3

Meßbereich	$\Delta\tau$ bei f_M =			$\Delta U/U_o$
	556/500 kHz	277/250 kHz	93/83 kHz	
Fehler-grenzen (e)	0.6 ns	1.2 ns	3.6 ns	0.25 %

Table 8-3

Key for Table 8-3:

Messbereich	=	Measuring range
Fehlergrenzen (e)	=	Error limits (e)
bei	=	with

- Increase test deviation Δf with potentiometer [16] (P 1501) at the RMS-4 to 300 kHz
- Adjust the test frequencies $f_M > 1$ MHz with the selection switch for the measuring frequency [19] (S 1501) at the RMS-4 and read off in each case the width of the noise result indication

Error limits (e) for $\Delta\varphi$: 0.25% rad

$\Delta U/U_o$: 0.25%

- Increase test deviation Δf to 500 kHz and lower IF send level P_1 to -20 dBm [at the RMS-4 switch [13] (EL 601) to -10 dBm and potentiometer [2] (P 1201) to -10 dB, at the RME-4 switch [31] (EL 701) to -10 dBm]
- Carry out measurement at each test frequency as described above

Error limts (e) for $\Delta\varphi$: 0.25% rad

$\Delta U/U_o$: 0.25%

8.2.2. Intrinsic Noise in the BB Plane

Measuring setup: Back-to-back measurement RMS-4 - RME -4
Connection between output [14] (Bu 1605) and input [30] (Bu 1901).

Advice: The back-to-back connection is to be established with the short 75 Ω cable supplied

Settings of the instrument:

RMS-4	[15]	(S 1601):	40 dB (both pushbuttons pressed)
	[16]	(P 1501):	-10 dBm
	[17]	(P 1305):	Right stop
RME-4	[29]	(S 1601):	Input BB - Distortion
	[33]	(S 1901):	Not pressed (-50 to -30 dBm)
	[34]	(S 1602):	U_x from BB
	[9]	(S 2203):	Pushbutton "$\Delta\varphi$, $\Delta\tau$" pressed
	[23]	(S 2204);	Pushbutton "$\Delta U/U_o$" pressed

10	(S 2205):	1 ns/0.5% rad
24	(S 2202):	0.5%
11	(S 601) :	6 kHz / 0 MHz

- Adjust visual unit so that the results $\Delta\tau$ or $\Delta\varphi$ and $\Delta U/U_o$ are visible
- Dial through measuring frequency selection switch 19 (S 1501) at the RMS-4 and read off the width of the noisy result indication; compare the results with Table 8-4

Meßbereich	$\Delta\tau$ bei f_M =			$\Delta\varphi$	$\Delta U/U_o$
	556/500 kHz	277/250 kHz	93/83 kHz	(bei f_M > 1 MHz)	
Fehler-grenzen (e)	0.6 ns	1.2 ns	3.6 ns	0.3% rad	0.3%

Table 8-4

Key for Table 8-4:

Messbereich	=	Measuring range
Fehlergrenzen (e)	=	Error limits (e)
bei	=	with

Changes in instrument settings:

RMS-4	15	(S 1601):	0 dB (both pushbuttons released)
	17	(P 1305):	0.1V
RME-4	33	(S 1901):	Pressed (-30 to -10 dBm)

- Dial through measuring frequency selections switch 19 (S 1501) at the RMS-4 and read off the width of the

noisy result indication; compare the results with Table 8-5

Meßbereich	$\Delta\tau$ bei f_M = 556/500 kHz	277/250 kHz	93/83 kHz	$\Delta\varphi$ (bei f > 1 MHz)	$\Delta U/U_o$
Fehler-grenzen (e)	0.3 ns	0.6 ns	1.8 ns	0.1 % rad.	0.1%

Table 8-5

Key for Table 8-5:

Messbereich	=	Measuring range
Fehlergrenzen (e)	=	Error limits (e)
bei	=	with

8.3. IF Frequency Response

8.3.1. IF Frequency Response ΔP_1

Measuring setup: Back-to-back measurement RMS-4 - RME-4
Connection between P_1-output [1] (Bu 1)
and P_1-input [27] (Bu 1)

Advice: The back-to-back connection is to be established with the short 75 Ω cable supplied

Settings of the instrument:

RMS-4	[2]	(P 1201):	-5 dB
	[13]	(EL 601):	+10 dBm
	[4]	(S 803):	70/140 MHz
	[7]	(S 1301):	off

	[8]	(S 902):	Sweep
	[9]	(S 903):	70 MHz
	[16]	(P 1501):	Left stop
	[17]	(P 1305):	25 MHz
	[18]	(S 801):	2 $\hat{\Delta F}$
	[20]	(S 1302):	70 Hz
RME-4	[29]	(S 1601):	Input IF
	[31]	(EL 701):	+10 dBm (tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	70 MHz
	[14]	(P 2203):	Right stop
	[9]	(S 2203):	Pushbuttons "ΔP_I" and "ΔP_{II}" pressed simultaneously ($\hat{=}$ high ΔP_I sensitivity)
	[11]	(S 601) :	6 kHz / 0 MHz

- Push the data line with potentiometer [8] (P 2201) at the RME-4 into the center of the CRT screen
- Read off intrinsic frequency response (= maximum deviations from an average value)

Limits of errors (e): ± 0.05 dB

- Switch IF at RMS-4 and RME-4 to 140 MHz (switch [9] (S 903) and [37] (S 1402)) and repeat measurement

Limits of errors (e): ± 0.1 dB

- Adjust IF send level P_I to -20 dBm (at RMS-4, set switch [13] (EL 601) to -10 dBm and potentiometer [2] (P 1201) to -10 dB, and at RME-4, set switch [31] (EL 701) to -10 dBm) and carry out measurements

Limits of errors (e) at 70 and 140 MHz ± 25 MHz: ± 0.1 dB

at 140 MHz ± 50 MHz: ± 0.2 dB

- Adjust IF send level P_I to +10 dBm (at RMS-4, set switch [13] (EL 601) to +10 dBm and potentiometer [2] (P 1201) to 0 dB; at RME-4, set switch [13] (EL 701) to +10 dBm) and carry out measurements

Limits of error(e) at 70 and 140 MHz ± 25 MHZ: ± 0.1 dB

at 140 MHz ± 50 MHz: ± 0.2 dB

8.3.2. IF Frequency Response ΔP_{II}

Measuring setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I-output [1] (Bu 1) and P_{II}-input [28] (Bu 1701) and connection between P_{II}-output [10] (Bu 502) and P_I-input [27] (Bu 1)

Advice: For the connection [1]-[28], the short 75 Ω cable supplied is to be used

Settings of the instrument:

RMS-4 [2] (P 1201): 0 dB

[13] (EL 701): -10 dBm

other settings as in Section 8.3.1.

RME-4 [31] (EL 701): 0 dBm (tracking)

[9] (S 2203): Pushbutton "ΔP_{II}" pressed

other settings as in Section 8.3.1.

- Shift data line with potentiometer [8] (P 2201) at the RME-4 into the center of the CRT screen

- read off intrinsic frequency response

Error limits (e): ± 0.25 dB (≙ 0.05 screen parts)

- Switch IF at RMS-4 and RME-4 to 140 MHz (switch [9] (S 903) and [37] (S 1402)) and repeat measurement

Error limits (e): ± 0.5 dB (≙ 0.1 screen parts)

- Adjust IF send level P_I to -50 dBm (at the RMS-4, set switch [13] (EL 601) to -40 dBm and potentiometer [2] (P 1201) to -10 dB) and carry out measurements at IF of 70 and 140 MHz

Error limits (e): as stated above

8.4. Return Loss

8.4.1. Return Loss at the IF Connections

Instruments required:

1 Radio-link measuring setup	from W&G
1 Return loss measuring bridge	from W&G
1 T-piece 75 Ω	

8.4.1.1. IF Input P_I

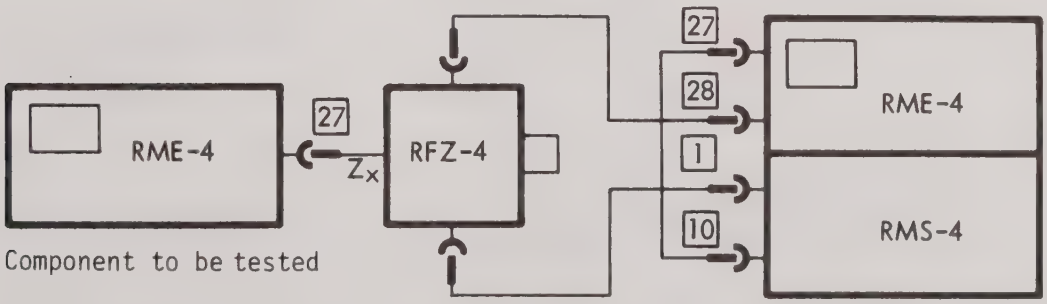


Fig. 8-3: Measuring setup for Section 8.4.1.1.

Setting of the instruments:

RME-4 (component to be tested)	31	(EL 701):	+10 dBm
RMS-4 (measuring setup)	2	(P 1201):	0 dB
	13	(EL 601):	-20 dBm
	7	(S 1301):	off
	8	(S 902):	Sweep
	9	(S 903):	70 MHz
	16	(P 1501):	Left stop
	17	(P 1305):	25 MHz (right stop)
	18	(S 801):	2 $\hat{\Delta}$F
	20	(S 1302):	70 Hz
RME-4 (measuring setup)	29	(S 1601):	Input IF
	31	(EL 701):	0 dBm (tracking)
	36	(S 1401):	Tracking
	37	(S 1402):	70 MHz
	9	(S 2203):	Pushbutton "ΔP_{II}" pressed
	14	(P 2203):	Right stop
	15	(S 1503):	Not pressed

Calibration:

- Operate measuring bridge RFZ-4 without component to be tested.
- At RME-4, adjust the display to the -30 dB screen line with potentiometer 8 (P 2201); for the measurement, this

reference line corresponds to a return loss a_r of 30 dB.

Measurement:

- Adjust send level at RMS-4 (measuring setup) to +10 dBm
- Connect Z_x terminal of the return loss measuring bridge directly with the P_I-input [27] (Bu 1) of the component to be tested
- Determine return loss for each divider position of [31] (EL 701) of the component to be tested and compare with with error limits in Table 8-6
- Switch IF at measuring setup RM-4 to 140 MHz; calibrate measuring bridge once again and repeat the a_r measurements as described above; compare data with the a_r values in Table 8-6

Anschluß	P_I [27]	
Bereich [31]	-10 dBm	0 dBm, +10 dBm
Geforderter a_r-Wert	≧26 dB	≧30 dB

Table 8-6

Key for Table 8-6:

Anschluss	=	Terminal
Bereich	=	Range
Geforderter a_r-Wert	=	a_r value required

8.4.1.2. IF Input P_{II}

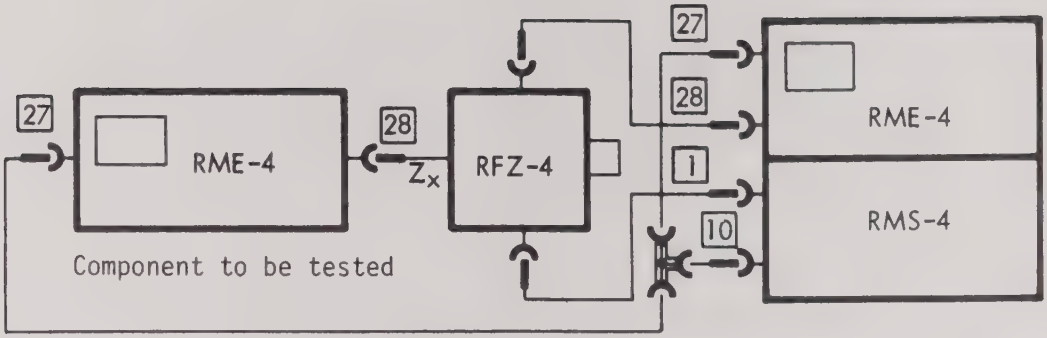


Fig. 8-4: Measuring setup for Section 8.4.1.2.

Settings of the Instruments:

RME-4 (component to be tested)	29	(S 1601):	Input IF
	31	(EL 701):	0 dBm (tracking)
	36	(S 1401):	Tracking
	37	(S 1402):	70 MHz
RMS-4 (measuring setup)	13	(EL 601):	-40 dBm

other settings as in Section 8.4.1.1.

RME-4 (measuring setup) settings as in Section 8.4.1.1.

Calibration:

- With send level setting at -40 dBm, calibrate as described in Section 8.4.1.1.

Measurements:

- Increase send levels at RMS-4 (measuring setup) to -10 dBm

- Connect Z_x terminal of the return los measuring bridge directly with the P_{II}-input [28] (Bu 1701) of the components to be tested
- Measure return loss: $a_r \geqq 26$ dB
- Switch IF at measuring setup and at component to be tested to 140 MHz; calibrate measuring bridge again and repeat a_r measurements as described above: $a_r \geqq 26$ dB

8.4.2. Return Loss of the BB Connections

Instruments required:

1 Level measuring setup	e.g. PSM-14	from W&G
1 Return loss measuring bridge	e.g. RFZ-5	from W&G

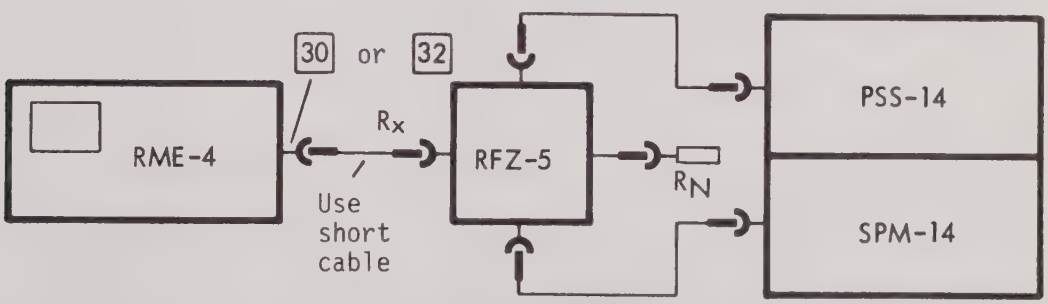


Fig. 8-5: Measuring setup for Section 8.4.2.

Settings of the instruments:

RME-4	29	(S 1601):	Input IF
	36	(S 1401):	Wide
PSS-14	send level ca. +8 dBm		
SPM-14	band width 360 Hz, low noise, f = 1 MHz		
RFZ-5	calibrated together with PSM-14, R_N = 75 Ω		

- Connect R_x terminal of the return loss measuring bridge with BB output 32 (Bu 501) of the RME-4 (use short cable!)
- Measure return loss at the test frequencies of 10, 80, 300 kHz, 1, 3, 10 and 13.6 MHz

$a_r \geqq 30$dB (error limits e)

- Now connect R_x terminal of the return loss measuring bridge with BB input 30 (Bu 1901) of the RME-4
- Measure return loss at test frequencies (setting at PSM-14), with which the RME-4, which is to be tested, is equipped with divider 33 (S 1901) keyed in or blanked out

$a_r \geqq 26$ dB (error limits e)

8.5. Absolute IF Level Measurement P_I

Instrument required:

1 Calibration level meter with sensing head and accessories	e.g. EPM-1 with from W&G TK-10

Measuring setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I-output [1] (Bu 1) and P_I-input [27] (Bu 1)

Settings of the instruments:

RMS-4	[2]	(P 1201):	0 dB
	[13]	(EL 601):	0 dBm
	[4]	(S 803):	70/140 MHz
	[8]	(S 902):	Sweep
	[9]	(S 903):	70 MHz
	[16]	(P 1501):	ca. 50 kHz
	[17]	(P 1305):	Left stop
RME-4	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	70 MHz
	[15]	(S 1503):	Pushbutton "Δf, P_I" pressed

EPM-1 Measuring range ± 0.2 dBm; TK-10 calibrated with 0 dBm, Z_{out} = 75 Ω

Calibrating the Level Indication

- With a send level of 0 dBm, make reference line (lower horizontal line) coincide with the -10 dB graticule line by using potentiometer [6] (P 309/St-1) and make the test line (upper horizontal line) coincide with the 0 dB graticule line by using potentiometer [21] (P 1306)

- Switch over to a send level of -10 dBm, check whether test and reference lines coincide with the -10 dB graticule line
- If this is the case, the calibration process is concluded
- If the test line does not fall on the -10 dB graticule line (which can happen as the result of ageing or of drift), the expansion should be recalibrated by potentiometer [21] (P 1306). A shift in the Y direction should be corrected with potentiometer [39] (P 1504).

  The two potentiometers are adjusted by alternately switching on send levels of 0 and -10 dBm, and this is to be repeated until the test lines of the two levels actually coincide with their respective graticule lines.

Level Measurement

- Connect the sensing head of the calibrating level meter with the P_I output [1] (Bu 1) of the RMS-4 and adjust the send level of the RMS-4 exactly to 0 dBm
- Re-establish connection between P_I output [1] (Bu 1) and P_I input [27] (Bu 1) and read off level at display unit

error limits (e): ± 0.6 dB

- Switch measuring setup RM-4 to wideband operation

(switch [8] (S 902) at RMS-4 and switch [36] (S 1401) at RME-4)

- Read off level at display unit

error limits (e): ± 0.8 dB

- Switch over measuring setup RM-4 to IF 140 MHz (switch [9] (S 903) at RMS-4 and switch [37] (S 1402) at RMS-4)
- Adjust send level of the RMS-4 exactly to 0 dBm with the help of the calibrating level meter and subsequently re-establish back-to-back connection between RMS-4 and RME-4
- With operating mode set to "sweep/tracking" and "wide band", read off level at display unit

error limits (e): ±0.5 dB in "sweep/tracking" operating mode
±0.6 dB in "wide band" operating mode

8.6. IF R.M.S. Deviation Measurement

Measuring setup: back-to-back measurement RMS-4 - RME-4
connection between P_I-output [1] (Bu 1) and
P_I-input [27] (Bu 1)

Settings of the instrument:

RMS-4	[2]	(P 1201):	0 dB
	[13]	(EL 601):	0 dBm
	[4]	(S 803):	70/140 MHz
	[8]	(S 902):	Sweep
	[9]	(S 903):	70 MHz
	[17]	(P 1305):	Left stop
	[19]	(P 1305):	0.277 or 0.250 MHz
RME-4	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)

RME-4 cont. [36] (S 1401): Tracking

[37] (S 1402): 70 MHz

[15] (S 1503): Pushbutton "Bessel" pressed

- Adjust deviation measurement Δf with potentiometer [16] (P 1501) at the RMS-4 so that the IF carrier, shown on the display unit, becomes zero and only the two side lines are still visible; in order to increase sensitivity, press pushbutton [20] (S 901) at the RME-4
- Read off set value at the scale of the potentiometer [16] (P 1501) and compare with the value in Table 8-7; the error limits given correspond with the specifications of the RMS-4: ± 15 kHz ± 0.08 Δf

Meßfrequenz f_M [19]	Soll-Meßhub Δf [16]	Fehlergrenzen (e) der Abweichung
277,7 kHz	472.4 kHz	±52.8 kHz
250 kHz	425.15 kHz	±49 kHz

Table 8-7

Key for Table 8-7:

Messfrequenz f_M [19]	=	Test frequency f_M [19]
Soll-Messhub Δf [16]	=	Nominal test deivation Δf [16]
Fehlergrenzen (e) der Abweichung	=	Error limits (e) of the deviation

- Do not change the measurement deviation setting found
- At the RME-4, press pushbutton"Δf; P_I" and release pushbutton "Bessel" [15] (S 1503)
- With potentiometer [5] (P 308), move the left vertical line until it coincides with the zero line of the graticule
- With potentiometer [13] (P 1304) move the test line (right vertical line) to coincide with the calibrating mark ∇ on the graticule disk
- At RMS-4, set the test deviation Δf to the 450 kHz scale value with potentiometer [16] (P 1501)
- With switch [19] (S 1501), dial all test frequencies and read off the deviations from 450 kHz on the display unit

error limits (e): $\pm$ 64.5 kHz ($\hat{=}$ the specifications of the RM-4: $\pm$ 11% v.M.$\pm$ 3% v.E.)

Check of the 2.5 MHz Test Range:

Changes in the Instrument Settings:

RMS-4:	[8]	(S 902):	Wideband
	[15]	(S 1601):	Push button not pressed
	[16]	(P 1501):	Left stop
RME-4:	[15]	(S 1503):	"Bessel" push button pressed
	[16]	(S 1301):	2.5 MHz

- At RMS-4, connect output [14] (Bu 1605) with input [11] (Bu 1606)
- Increase test deviation ΔF with potentiometer [16] (P 1501) at RMS-4 until the second (third, fourth) zero passage of the carrier has been set accurately; to increase sensitivity, press pushbutton [20] (S 901) at RME-4
- Thereafter release push button "Bessel" and press push button "ΔF; PI" [15] (S 1503), place switch [36] (S 1401) in "Wideband" position, read the r.m.s. deviation on the CRT screen of the display unit and compare with the values in Table 8-8; the given error limits correspond to the RM-4 specifications: ± 7 % of reading ± 3 % full scale deflection.

Note: For adjusting the zero crossing in mode "Bessel", the switch [36] should be switched to "Tracking" position.

	Meßfrequenz f_M [19]	Soll-Meßhub Δf [16]	Fehlergrenzen (e) der Abweich. in kHz	in Rasterteilen
2. Trägernull-durchgang	277.7 kHz 250 kHz	1084.2 kHz 975 8 kHz	±150.9 ±143.3	±0.6 ±0.57
3. Trägernull-durchgang	277.7 kHz 250 kHz	1699.8 kHz 1529.8 kHz	±194.0 ±182.1	±0.78 ±0.73
4. Trägernull-durchgang	277.7 kHz 250 kHz	2316.2 kHz 2084.6 kHz	±237.1 ±220.9	±0.95 ±0.88

Table 8-8

Key for Table 8-8:

Messfrequenz	=	Test frequency
Soll-Mess-hub	=	Nominal test deviation
Fehlergrenzen (e) der Abweich.	=	Error limits (e) of the deviations
in Rasterteilen	=	In graticule divisions
2. Trägernull-durchgang	=	Second zero passage of the carrier
3.	=	Third
4.	=	Fourth

8.7. Sweep Deviation Measurement

Measurement Set Up: Back-to-back measurement RMS-4 - RME-4

Connection between P_I output [1] (Bu 1)

and P_I input [27] (Bu 1)

Settingsof the instruments:

RMS-4:	[2]	(P 1201):	0 dB
	[13]	(EL 601):	0 dBm
	[4]	(S 803):	70/140 MHz
	[7]	(S1301):	off
	[8]	(S 902):	Sweep
	[9]	(S 903):	70 MHz
	[16]	(P 1501):	Left stop
	[17]	(P 1305):	18 MHz
	[18]	(S 801):	2 $\hat{\Delta}$F
	[20]	(S1302):	70 Hz
RME-4:	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[36]	(S 1401):	Tracking

[37]	(S 1402):	70 MHz
[2]	(S 2201):	~
[9]	(S 2203):	Pushbutton "ΔP_I" depressed
[11]	(S 601):	5 MHz
[18]	(P 1502):	ca. mid-position
[14]	(P 2203):	Right stop
[40]	(S 1501) :	≂

- Set variable frequency markers M 1 and M 2 with potentiometers [25] (P 1610) and [26] (P 1611) accurately to start and end of image, so that they barely light üp at the edge of the image.
- slowly widen sweep width $\hat{\Delta F}$ at RMS-4 with potentiometer [17] P 1305) until the 20 MHz frequency marker (4th mark from the center pf screen) appears et the edge of the CRT screen. Now this must be brought to exact coincidence with marks M 1 or M 2.
- with this setting, read off the deviation from 20 MHz at the scale of potentiometer [17] (P 1305); the deviations must be determined at the start and at the end of the image, because these values may be different.
- error limits (e): $\pm$1.9 MHz ($\hat{=}$ the combination of specifications: 2% of full-scale deflection $\pm$0.05 X $\hat{\Delta F}$ at RMS-4 and $\pm$0.01 X $\hat{\Delta F}$ at RME-4)
- switch IF at RM-4 to 140 MHz (switch [9] (S 903) at RMS-4 and switch [37] (S 1402) at RME-4) and repeat measurement (Note: the actual values now are twice the scale values at potentiometer [17] (P 1305) of the RMS-4)
  error limits (e): $\pm$3.8 MHz

8.8. Noise Properties

Instruments Required:

1 White noise measuring set up	e.g. RK-50	from W&G
2 Band limiting filters for 1800 and 2700 channel systems	e.g. RSB-316/8160 and RSB-316/12360	from W&G
6 Band-stop filters for the test frequencies 534, 1248, 2438, 5340, 7600 and 11700 kHz	e.g. RSS-534,..., RSS-11700	from W&G
6 Converter plug-ins for the test frequencies given above	e.g. REU-534,..., RSS-11700	from W&G
2 Pre-emphasis networks for 1800 and 2700 channel systems	e.g. pre-emphasis networks BN 445/12 and BN 445/13	from W&G
2 De-emphasis networks for 1800 and 2700 channel systems	e.g. de-emphasis networks BM 446/12 BN 446/13	from W&G

1 Attenuator 5dB, Z = 75Ω

1 Remote control cable K 176 (not absolutely required, simplifies operation)

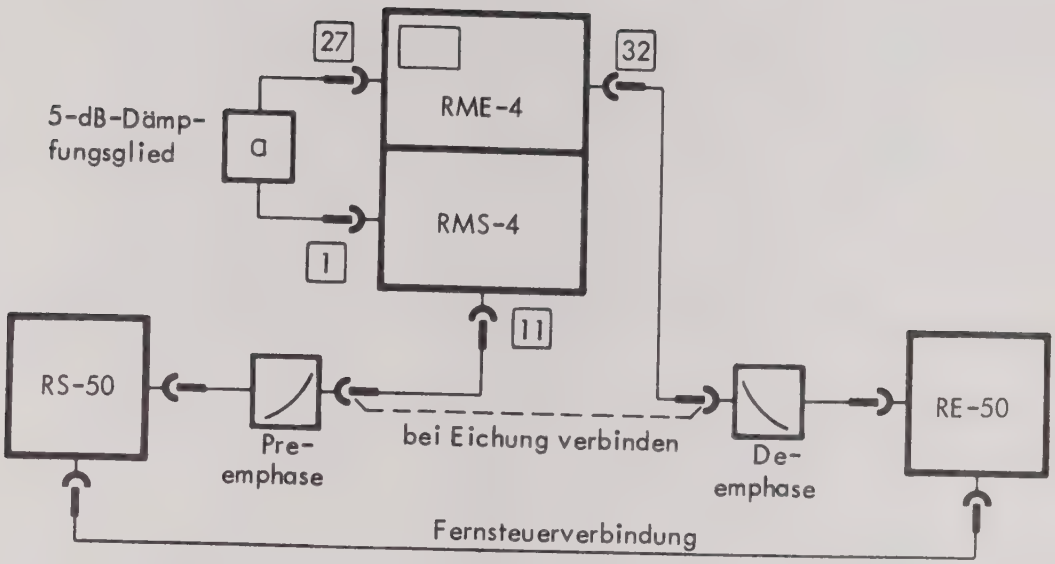


Figure 8-6: Measuring Setup For Section 8.8.

Key For Figure 8-6:

Dämpfungsglied	=	Attenuator
Pre-emphase	=	Pre-emphasis
bei Eichung verbinden	=	Connect for calibration
De-emphase	=	De-emphasis
Fernsteuerverbindung	=	Remote-control connection

Settings of the Instruments:

RMS-4:	2	(P1201):	-5dB
	13	(EL 601):	+10 dBm
	4	(S 803):	70/140 MHz
	8	(S 902):	Wideband
	9	(S 903):	70 MHz
	34	(S 901):	intern
RME-4:	29	(S 1601):	Input IF
	31	(EL 701):	0 dBm (Wideband)
	36	(S 1401):	Wideband
	37	(S 1402):	70 MHz

RS-50: Send level -3.2 dBm, band-stop filters off
band limiting filter RSB-316/8160

RE-50: S/N channels ≧240, Rel. level -29.6 dBr
test range "▼"

- Connect pre-emphasis and de-emphasis networks directly with one another
- Dial through all test channels at the white noise receiver; if the settings are correct, the pointer of the instrument should point to the marker "▼"; note any deviations and take into consideration the correct sign later when measuring (in so doing, it is advantageous if the deviations are noted in dB)
- Connect pre-emphasis and de-emphasis networks at the RMS-4 or RME-4, switch on the band-stop filters at the noise level sender and switch the measuring range at the white noise receiver to -70 dBm0p
- Carry out measurements in all test channels, with the exception of 11700 kHz, according to Table 8-9

Messung	1800 Kanäle / ZF 70 MHz		
	Sendepegel	Erlaubte Geräuschwerte	
Grundgeräusch	aus	≦20 pW0p	≦-77 dBm0p
Grund- u. Intermodulationsgeräusch bei Nennlast	-3.2 dBm	≦40 pW0p	≦-74 dBm0p
Grund- u. Intermodulationsgeräusch bei 3 dB Überlast	-0.2 dBm	≦60 pW0p	≦-72.2 dBm0p
Bandbegrenzungsfilter RSB	RSB-316/8160		
Pre- u. Deemphase	1800 Kanäle		

Table 8-9

Key For Tables 8-9 & 8-10

Messung	=	Measurement
Kanale	=	Channels
Sendepegel	=	Send level
Erlaubte Geräuschwerte	=	Permissible noise values
Grundgeräusch	=	Background noise
aus	=	off
Grund- u. Intermodulationsgeräusch bei Nennlast	=	Background and intermodulation noise under normal load
Grund- u. Intermodulationsgeräusch bei 3 dB Überlast	=	Background and intermodulation noise under an overload of 3 dB
Bandbegrenzungsfilter RSB	=	Band limiting filter RSB
Pre- u. Deemphase	=	Pre-emphasis and de-emphasis

- Repeat measurements at IF 140 MHz in all test channels corresponding to Table 8-10

Messung	2700 Kanäle / ZF 140 MHz		
	Sendepegel	Erlaubte Geräuschwerte	
Grundgeräusch	aus	≦35 pW0p	≦-74.5 dBm0p
Grund- u. Intermodulationsgeräusch bei Nennlast	-1.5 dBm	≦50 pW0p	≦-73 dBm0p
Grund- u. Intermodulationsgeräusch bei 3 dB Überlast	+1.5 dBm	≦80 pW0p	≦-71 dBm0p
Bandbegrenzungsfilter RSB	RSB-316/12360		
Pre- und Deemphase	2700 Kanäle		

Table 8-10

8.9. Modulation Frequency Response

8.9.1. Measurement in the Frequency Range 10 kHz to 13.6 MHz

Instruments required:

1 Level measuring setup e.g. PSM-14 from W&G

1 Attenuator 6 dB, Z = 75Ω

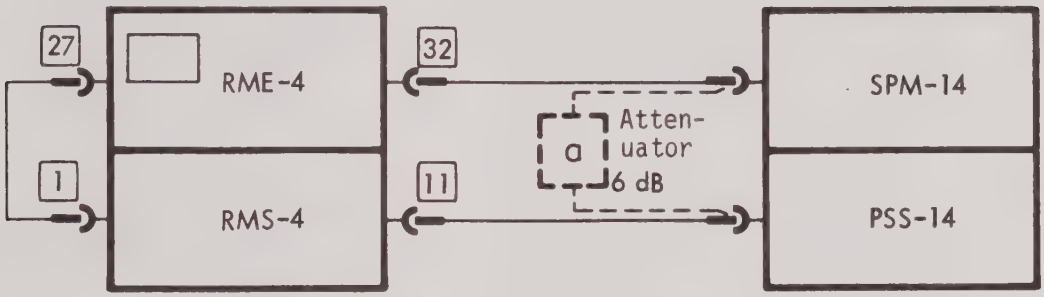


Figure 8-7: Measuring setup for Section 8.9.1.

Settings of the Instruments:

RMS-4:	2	(P 1201):	0 dB
	13	(EL 601):	0 dBm
	4	(S 803):	70/140 MHz
	8	(S 902):	Wideband
	9	(S 903):	70 MHz
	34	(S 901):	intern
RME-4:	29	(S 1601):	Input IF
	31	(EL 701):	0 dBm (wideband)
	36	(S 1401):	Wideband
	37	(S 1402):	70 MHz

PSS-14: Level setting ca. -20 dB

SPM-14: Wideband 360 Hz, test range -26 dB, expanded display

- Record intrinsic frequency response of the level measuring setup with 6 dB attenuator inserted
- Measure modulation frequency response of the measuring setup RM-4 in the frequency range 10 kHz to 10 MHz, taking into consideration the intrinsic frequency response of the level measuring setup; the measured frequency response is to be compared with the error limits in Table 8-11
- Carry out measurement also at IF = 140 MHz

ZF ([9],[37])	Frequency range	Error limits (e) relative to 1 MHz
70 MHz	10 kHz bis 10 MHz	±0.5 dB
140 MHz	10 kHz bis 13.6 MHz	±0.5 dB

Table 8-11

- For the VLF measurement, the deviation at 10 kHz should be determined separately according to Section 8.9.2.

8.9.2. Measurement in the Frequency Range 50 Hz to 10 kHz

Instruments Required:

1 VLF test instrument e.g. PMG-2 from W&G

1 Attenuator 6 dB, Z = 75Ω

1 Series resistance 75Ω

1 Terminating impedance 75Ω

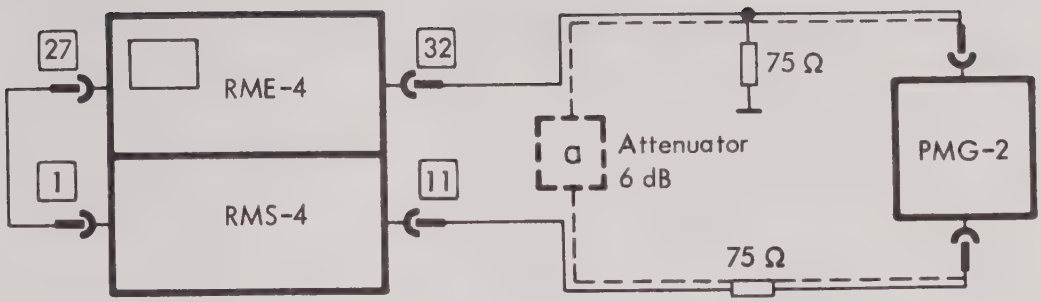


Figure 8-8 Measuring setup for Section 8.9.2.

Settings of the Instruments:

RMS-4 and RME-4: as in Section 8.9.1

PMG-2: Send level ≦ -13 dB, Z_{out} = approx. 0 Ω

Receiver level range: -20 dB, display range +1 to -5 dB,

$R_{input} \approx 50\ k\Omega$

- Record intrinsic frequency response of the VLF measuring instrument with the 6dB attenuator inserted
- Measure modulation frequency response of the measuring setup RM-4, taking into consideration the intrinsic frequency response of the VLF measuring instrument
- Subsequently correct all values by the data obtained in Section 8.9.1. at f = 10 kHz

  Error limits (e) relative to 1 MHz: $\pm$0.5 dB
- Repeat measurement at IF 140 MHz

  Error limits (e) relative to 1 MHz: $\pm$0.5 dB

8.10 BB LEVEL MEASUREMENT

General information: Measurements should not be made before at least 1 hour warming-up time and the ambient temperature should be 23°C $\pm$ 3°C.

The errors are stated as operating errors in various frequency bands in the Specifications (Section 1.4). The tests selected here include the most important partial errors that are determined by these specified values.

8.10.1. DEFECTS IN LEVEL INDICATION AT -30 dBm

Instruments required:

1 Level Generator	e.g. PS-14/BN 834	supplied by W&G
1 Milliwatt Power Meter with accessory	e.g. EPM-1/BN 564 (TK-10)	supplied by W&G
1 variable calibrated attenuator	e.g. D 120	supplied by Siemens

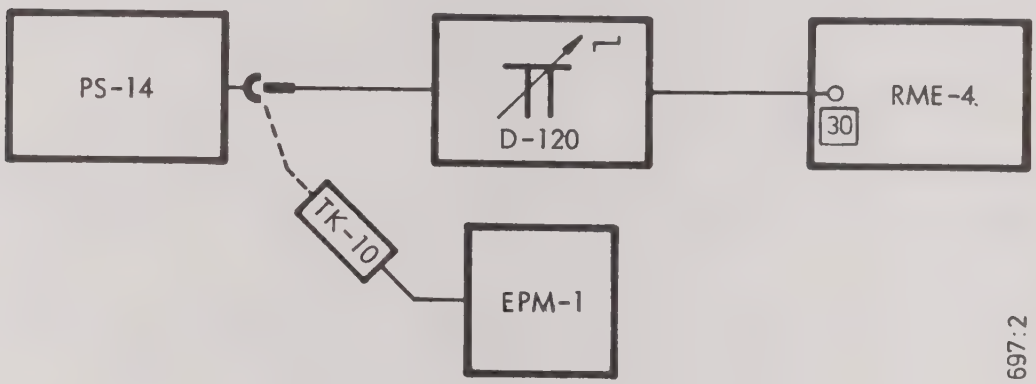


Figure 8-9 Measuring set-up for Section 8.10.1

Settings:

EPM-1: Measuring range ±0.2 dBm
TK-10 calibrated at 0 dBm, R_i = 75Ω

PS-14: f = 100 kHz
output level = set precisely at 0 dBm using EPM-1/TK-10
(connection shown by broken line)

D-120: Set attenuation at 30.00 dB

RME-4: Switch [29] (S 1601) BF level, P_{BF}

Test component: Switch [42] (S 3201) CAL

Calibrate the BF level meter to -30.00 dBm using the Potentiometer [41] (P 3203) "CAL". Then move switch [42] to the middle setting "P_{BF}. Produce measuring setup as illustrated above. Read off deviation from 30.00 dBm from the display.

Error limit (e): ± 0.04 dB

8.10.2. ATTENUATOR ERRORS AND FREQUENCY RESPONSE INFLUENCE

Instruments required:

1 Level Generator	e.g. PS-14/BN 834	supplied by W&G
1 Milliwatt Power Meter with accessories	e.g. EPM-1/BN 564 (TK-10 and T-piece BN 595/1)	supplied by W&G
1 variable calibrated attenuator	e.g. D-120	supplied by Siemens

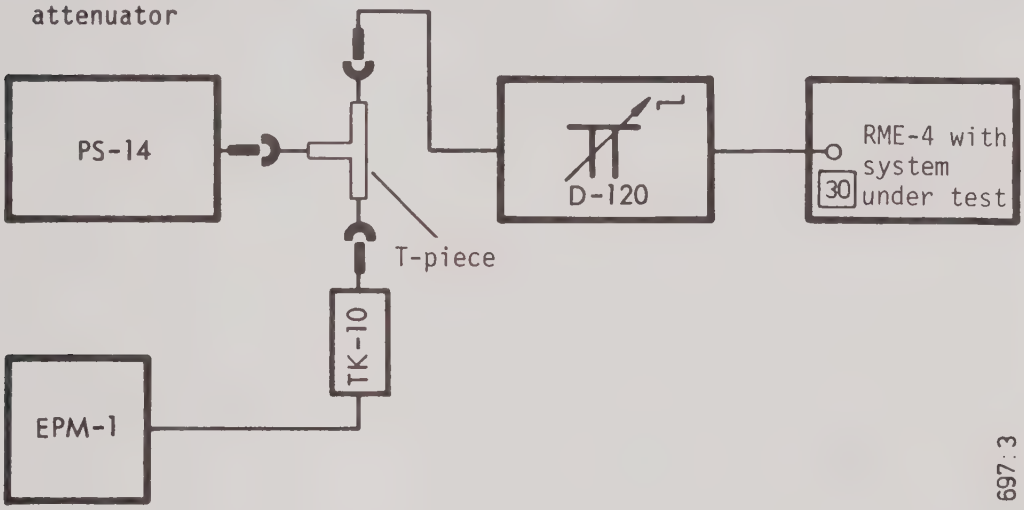


Figure 8-10 Measuring set-up for Section 8.10.2.

Settings:

EPM-1: Measuring range ±0.2 dBm
TK-10 calibrated at 0 dBm, Z_{out} = 75Ω

PS-14: f = 100 kHz
output level = set at approximately 6 dBm so that EPM-1 indicates exactly 0 dBm.

RME-4: Switch [29] (S 1601) BF level, P_{BF}

(System under Test) Switch [42] P_{BF}

Adjust attenuation of the calibrated attenuator so that the BF level meter indicates exactly -30.00 dBm (if necessary, readjust using potentiometer [41] CAL.). Record the appropriate attenuation of the calibrated attenuator as a reference value. Starting from this reference value, turn the calibrated attenuator through steps of 1, 2, 4, 6, 8, 10 and 20 dB, both to reduce and increase attenuation. At each step adjust the level of the generator within the specified frequency range

and at the same time note the indication on the BF Level Meter. The maximum deviations on the set value (= -30 dBm + $\Delta a_{\text{calibrated attenuator}}$) should be determined in each case. Any natural frequency response of the level meter (can be read on the EPM-1) should be taken into account here.

Error limits (e)	In frequency range 50 kHz...1 MHz	12 kHz...14 MHz
For above settings	± 0,09 dB	± 0,31 dB
For any other settings	± 0,14 dB	± 0,36 dB

8.10.3. RETURN LOSS

Measuring instruments required:

1 Return Loss Measuring Bridge — e.g. RFZ-5/BN 394 — supplied by W&G

1 Level Measuring Setup — e.g. PSM-14/BN 830, 833 — supplied by W&G

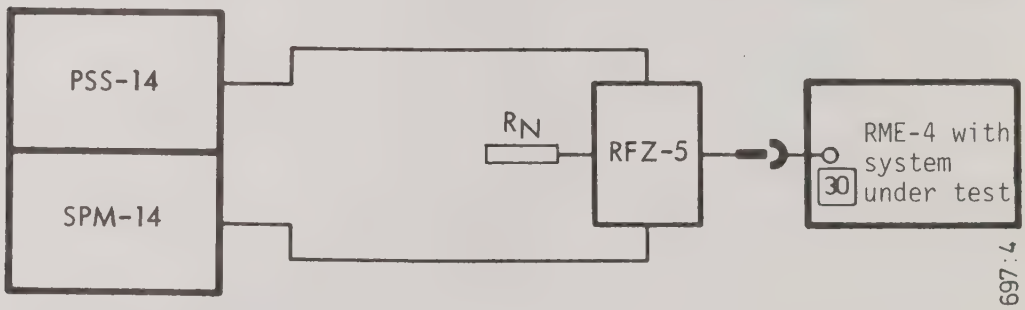


Figure 8-11 Measuring set-up for Section 8.10.3.

Settings:

RFZ-5: Calibrated together with PSM-14, R_N = 75 Ω

PSS-14: Output level approximately +8 dBm

SPM-14: Bandwidth 360 Hz
low noise setting
f = 1 MHz

RME-4: (System under Test) Switch [29] (S 1601) BF level, P_{BF}
Switch [42] (S 3201) P_{BF}

The return loss should be determined in the complete frequency range from 12 kHz to 14 MHz.

Error limit (e) $a_r \geq 26$ dB

9. INSTRUCTIONS FOR MAKING ADJUSTMENTS

An adjustment is required if a repair has been carried out on the RME-4 or if the check of the technical data, described in Chapter 8, has revealed that error limits are exceeded. This Chapter provides information concerning the adjustments required in this case.

Unless stated otherwise, all adjustments should be carried out at room temperature (+23°C ±3°C) and after a warming-up period of 30 minutes.

Because of the appreciable cost of measuring and testing equipment, it is not possible for the user to adjust the demodulator component [27]. Procedures to be followed have already been described in the introduction to Chapter 7, ADVICE FOR TROUBLESHOOTING.

If possible, the covers for the screen should remain on the printed circuits during the adjusting work, because the adjusting elements generally are accessible through boreholes in the frame of the tub or in the cover for the screen.

In the case of back-to-back measurements with RMS-4 and RME-4, care must be taken that the instruments, which belong together, are used for the measurement. The information, required for this purpose, may be found on the rear panel of the instrument.

9.1. Adjusting the Supply Voltages

Instrument required:

1 Digital voltmeter e.g. 8000 A of Fluke

Versorgungs-spannung	gemessen an	auf Platine	Abgleich mit
+12 V ±60 mV	R 109	697-BA	P 101
-24 V ±48 mV	C 111 (-)	697-BA	P 102
+5 V ±25 mV	R 512	844-AA	P 501
+12 V ±60 mV	R 1209	844-A	P 1201
-12 V ±60 mV	C 1215 (-)	844-A	P 1202

Table 9-1: Adjustment of Supply Voltages

Key for Table 9-1:

Versorgungs spannung	=	Supply Voltage
gemessen an	=	measured at
auf Platine	=	on Board
Abgleich mit	=	Adjustment with

9.2. Adjustment of the ΔP_I Measuring Setup Intrinsic Frequency Respons

Before adjusting the ΔP_I measuring setup intrinsic frequency response, the frequency response of the RMS-4 send signal at the P_I output must be checked (see also service instructions for RMS-4, Section 8.2.).

If the send frequency response remains within the specified tolerances, the measuring setup frequency response must be adjusted according to Section 9.15.6.

9.3. Adjustment of the 10 dB Level Jump in the Case of the Absolute Level Measurement P_I

Instrument required:

1 Calibrating level meter with sensing head and accessories:	e.g. EPM-1 with TK-10	from W&G

Measuring setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I output [1] (Bu 1)

and P_I input [27] (Bu 1)

Settings of the Instruments:

RMS-4:	[2]	(P 1201):	0 dB
	[13]	(EL 601):	0 dBm
	[4]	(S 803):	70/140 MHz
	[8]	(S 902):	Sweep
	[9]	(S 903):	70 MHz
	[16]	(P 1501):	ca. 50 kHz
	[17]	(P 1305):	Left stop
RME-4:	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	70 MHz
	[15]	(S 1503):	Pushbutton "Δf; P_I" pressed

EPM-1: Measuring range $\pm$0.2 dBm; TK-10 calibrated with 0 dBm; $Z_{out} = 75\,\Omega$

- With the calibrating level meter, set the IF send level of the RMS-4 at socket [1] (Bu 1) to 0 dBm $\pm$0.02 dB
- Reconnect P_I sockets of RMS-4 and RME-4
- With potentiometer [6] (P 309/ST-1), set the reference trace ($\hat{=}$ lower horizontal beam trace) to the -10 dB graticule line of the graticule plate.
- Then set the test trace on the 0 dB graticule line with potentiometer [21] (P 1306)

- By changing over the RME-4 calibrated attenuator with switch [31] (EL 701) between 0 and +10 dBm adjust the 10 dB level jump of the test trace with the potentiometers [21] (P 1306), = expansion setting and [39] (P 1504) = Y shift to the 0 and -10 dB lines on the graticule.

9.4. Adjustment of the P_{II} Measuring Setup Intrinsic Frequency Response

Measuring Setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I output [1] (Bu 1) and P_{II} input [28] (Bu 1701) and connection between P_{II} output [10] (Bu 502) and P_I input [27] (Bu 1)

Advice: The short 75Ω cable is to be used for the connection [1] - [28].

Settings of the Instruments:

RMS-4:	[2]	(P 1201):	0 dBm
	[13]	(EL 601):	-10 dBm
	[4]	(S 803):	70/140 MHz
	[7]	(S 1301):	off
	[8]	(S 902):	Sweep
	[9]	(S 903):	70 MHz
	[16]	(P 1501):	Left stop
	[17]	(P 1305):	25 MHz
	[18]	(S 801):	$2\hat{\Delta}F$

	[20]	(S 1302):	70 Hz
RME-4:	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	70 MHz
	[14]	(P 2203):	Right stop
	[9]	(S 2203):	Pushbutton " ΔP_{II}"
	[11]	(S 601) :	6 kHz / 0 MHz

- Shift test-result trace to center of CRT screen with potentiometer [8] (P 2201) on RME-4
- With trimmer C 1703 on board [697-AV...] and IF of 70 and 140 MHz, adjust so that the frequency responses lie within the specified error limits.

  70 MHz $\pm$25 MHz: (e) = $\pm$ 0.25 dB
  140 MHz $\pm$50 MHz: (e) = $\pm$ 0.50 dB

9.5. Adjustment of the Logarithmizer Characteristic Line in the Case of the ΔP_{II} Measurement

Instruments Required:

1 Digital Voltmeter e.g. 8600 A from Fluke

1 20 dB Attenuator, Z = 75Ω

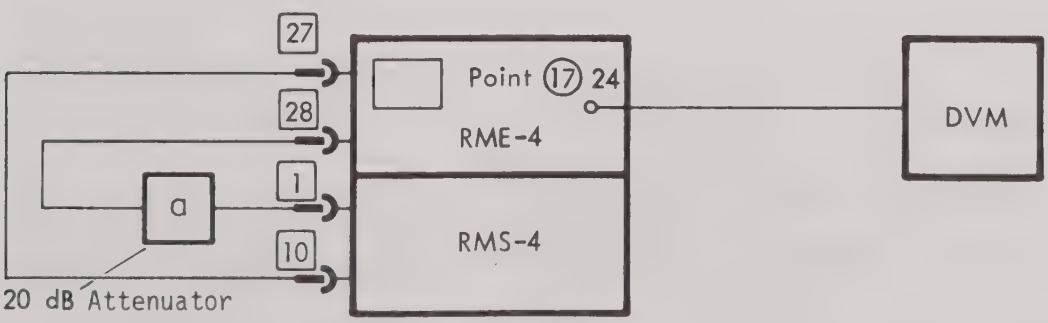


Figure 9-1: Measuring Setup for Section 9.5.

Settings of the Instruments:

RMS-4:	[2]	(P 1201):	-10 dB
	[13]	(EL 601):	-40 dBm
	[4]	(S 803):	70/140 MHz
	[7]	(S 1301):	off
	[8]	(S902):	Sweep
	[9]	(S 903):	140 MHz
	[16]	(P 1501):	Left stop
	[17]	(P 1305):	0.5 MHz
	[18]	(S 801):	off
	[20]	(S 1302):	70 Hz
RME-4:	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	140 MHz
	[11]	(S 601) :	6 kHz / 0 MHz

- Connect digital voltmeter to connection point (17) 24 of the board of the 20 MHz logarithmizer [697-AX] (use adapter card [697-AT] !)
- With trimmer C 1727, adjust the 20 MHz oscillating circuit on board [697-AW...] to the maximum output voltage (positive value)
- Set send level at RMS-4 to -10 dBm (switch [13] (EL 601) to 0 dBm) and with potentiometer P 1703 on board [697-AX] set an output voltage of 0 V
- Decrease send level of the RMS-4 with switch [13] by 20 dB and set the output voltage at connection point (17) 24 with potentiometer

P 1701 on board [697-AX] to - 160 mV ± 1 mV

- Decrease send level once again by 10 dB and set the output voltage with potentiometer P 1704 (board [697-AX]) to -240 mV ±1 mV
- In order to adjust the characteristic curve of the logarithmizer in the upper range, set send level at RMS-4 to +10 dBm and with potentiometer P 1702 on board [697-AX] set the output voltage at connection point (17) 24 to 160 mV ± 4 mV
- Set send level at RMS-4 to -10 dBm and with potentiometer P 1703 set the output voltage at connection point (17) 24 to 0 V ±20 mV
- The slope of the logarithmizer can be controlled on the CRT screen of the display unit by the representation of 10 dB level jumps. If necessary, it can be corrected with potentiometer P 1701.

9.6. Adjustment of the Return Loss at the IF Input P_{II}

Instruments Required:

1 Radio-link measuring setup RM-4 from W&G

1 Return loss measuring bridge RFZ-4 from W&G

1 T-piece 75 Ω

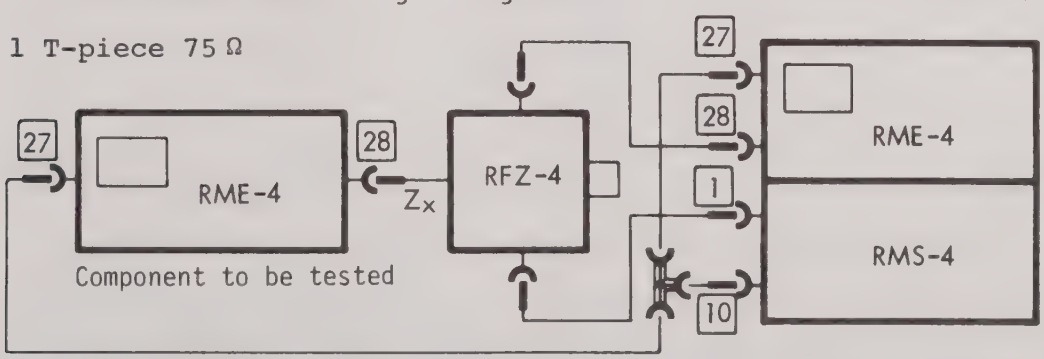


Figure 9-2: Measuring Setup for Section 9.6.

Settings of the Instruments:

RME-4 (Component to be tested)	29	(S 1601)	Input IF
	31	(EL 701):	0 dBm (tracking)
	36	(S 1401):	Tracking
	37	(S 1402):	140 MHz
RMS-4 (Measuring setup)	2	(P 1201):	0 dB
	13	(EL 601):	-40 dBm
	7	(S 1301):	off
	8	(S 902):	Sweep
	9	(S 903):	140 MHz
	16	(P 1501):	100 kHz
	17	(P 1305):	25 MHz
	18	(S 801):	2 $\hat{\Delta F}$
	19	(S 1501):	12.39 MHz
	20	(S 1302):	70 Hz
RME-4 (Measuring setup)	29	(S1601):	Input IF
	31	(EL 701):	0 dBm (tracking)
	36	(S 1401):	Tracking
	37	(S 1402):	140 MHz
	9	(S 2203):	Pushbutton " ΔP_{II}" presse
	14	(P 2203):	Right stop
	15	(S 1503):	Not pressed

Calibration:

- Operate measuring bridge RFZ-4 without component to be tested
- At RME-4, set the display on the -30 dB graticule line with potentiometer 8 (P 2201); in the measurement, this reference line corresponds to a return loss damping a_r of 30 dB

Measurement and Adjustment:

- Raise send level at RMS-4 (measuring setup) to -10 dBm
- Connect Z_x terminal of the return loss measuring bridge directly with the P_{II} input [28] (Bu 1701) of the component to be tested
- Adjust return loss to a maximum by changing the length of the wire of L 1708 (board [697-AV...]); the value required is $a_r \geqq 28$ dB
- Switch over IF at measuring setup and component to be tested to 70 MHz and check return loss (repeat calibration!) $a_r \geqq 28$ dB

9.7. Adjusting the Accuracy of Measurement in the Case of the Distortion Measurements $\Delta U/U_o$ and $\Delta\varphi$ or $\Delta\tau$

Instruments Required:

1 Level measuring set up	e.g. PSM-14	from W&G
1 2-way switch	e.g. REV-56	from W&G

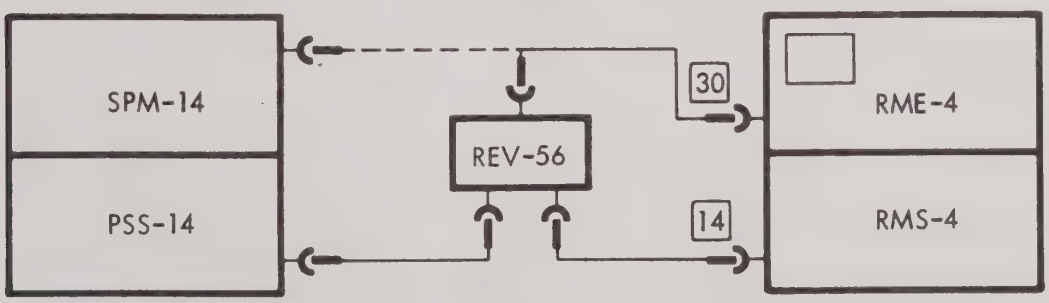


Figure 9-3: Measuring Setup for Section 9.7.

Settings of the Instruments:

RMS-4:	[15]	(S 1601):	Both pushbuttons pressed (≙ 40 dB)
	[16]	(P 1501):	Left stop
	[17]	(P 1305):	5 V (Right stop)

	[7]	(S 1301):	off
	[19]	(S 1501):	2.4 MHz
	[20]	(S 1302):	70 Hz
RME-4:	[29]	(S 1601):	Input BB (Distortion)
	[33]	(S 1901):	Pressed (-30...-10 dBm)
	[34]	(S 1602):	U_x from BB
	[2]	(S 2201):	≂ (calibration lines or
	[9]	(S 2203):	Pushbutton "$\Delta\varphi,\Delta\tau$" pressed
	[10]	(S 2205):	5% rad
	[23]	(S 2204):	Pushbutton "$\Delta U/U_o$" presse
	[27]	(S 2202):	5%
	[11]	(S 601) :	6 kHz / 0 MHz

PSS-14: Level setting 0 dBm

SPM-14: Width of band 360 Hz, test range - 10 dBm, expanded display

Warming up period for the measuring setup: ca 0.5 h!

Preparatory Settings:

- Initially, connect the output lead of the REV-56 with the level meter
- Set the level measuring setup to the test frequency f_M selected at the RMS-4 and read off level indication at level meter (ca. -10 dBm)
- Blank level sender and instead set the test voltage U_M at the RMS-4 with potentiometer [16] (P 1501) so that the same indication results at the level meter as in the step before (for this purpose, release pushbuttons [15]). At the same time, the level meter is to be tuned exactly to the test frequency (= level maximum). For the selected test frequency,

the test and auxiliary voltages are now the same in magnitude.

Note: With BB Level Meter equipped instruments, the test voltage and the auxiliary voltage can be set to equal values by use of this integral level meter. For this purpose, switch [29] is switched to the "BB Level" position.

Measurement:

- Connect 2-way switch with the BB input [30] (Bu 1901) of the RME-4
- Set auxiliary voltage at level sender to -38.06 dBm
- Adjust frequency $f_M + 2\ f_A$ at the level measuring setup. When the adjustment has been made correctly, a sinusoidal signal with a whole period is seen on the CRT screen of the display unit (at the same time, cross-fader [14] (P 2203) is at the left stop). If the frequency tuning is altered a little, a series of slightly displaced waves appear. The enveloping curve of the waved formed resembles a circle (see Figure 9-4)

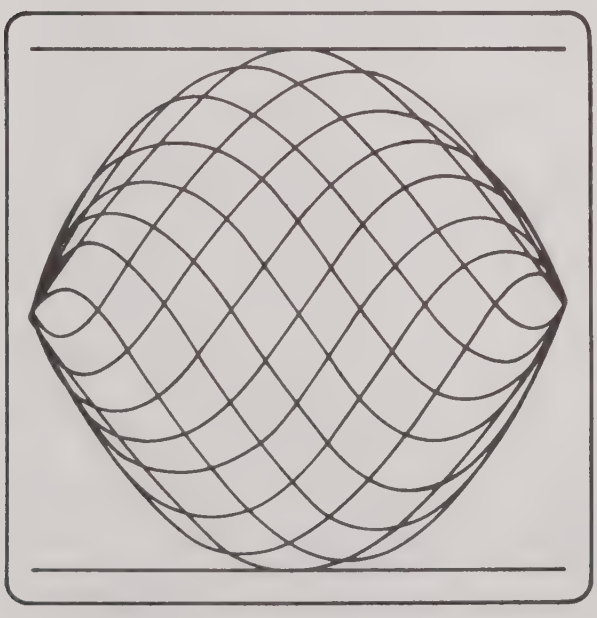


Figure 9-4

- The highest and lowest points of this circle ought to just touch the calibration lines. To achieve this, the auxiliary voltage at the Level Generator as well as the zero position on the CRT screen are altered with potentiometers [22] (P 2202) at "$\Delta U/U_o$" or [8] (P 2201) at "$\Delta\varphi, \Delta\tau$".

- After the adjustment has been made, read off level value at level sender. Determine deviation from the nominal value and compare with the error limits (e).

  Error limits (e): +0.83 dB / -0.92 dB } (corresponds to the specifications of the RME-4: ±10%)

- Then determine the deviation for the $\Delta\varphi$ result
- If the deviations are larger than the permissible error limits, the following adjustment must be carried out:
  Once again set the rated level of -38.06 dBm at the level sender; on board [697-AL] or [697-CB] adjust the peak value of the respective result shown so as to coincide with the calibration line, using potentiometer P 2209 (for $\Delta U/U_o$ results) and P 2210 (for $\Delta\varphi$ results).

9.8. Adjusting the Distance Between the Calibration Lines on the CRT Screen

Instruments Required:

1 Digital voltmeter	e.g. 8600A	from Fluke
1 DC voltage stabilizer	e.g. GS-1	from W&G

Settings at the RME-4: [2] (S 2201): ~ (calibration lines off)

- Raise plug-in card [697-AL...] or [697-CB...] by means of adaptor card [697-AT] or remove plug-in card [697-AU...] from

RME-4, so that the components of the plug-in card [697-AL...] or [697-CB...] become accessible

- Connect digital voltmeter to the cross-fader output, male connector - connection point 6 of board [697-AL...] or [697-CB...]
- Connect the base of T 2225 to -12 V via a 5 kΩ resistor, connect the collector from T 2224 to the chassis (taking care to use shortest path!)
- Establish a short circuit between TP 2201 and TP 2202 (base emitter T 2226)
- Set indication of the digital voltmeter to -200 mV $\pm$ 0.5 mV with potentiometer P 2205
- Remove short circuit between TP 2201 and TP 2202 and instead produce short circuit between TP 2202 and TP 2203 (base emitter JC 2204/5.2)
- Set indication of digital voltmeter to +200 mV $\pm$ 0.5 mV with potentiometer P 2204
- Remove short circuit between TP 2202 and TP 2203 as well as between collector T 2224 and chassis, disconnect -12 V from connection point 5
- Connect P_I output [1] (Bu 1) of the RMS-4 with P_I input [27] (Bu 1) of the RME-4

Settings of the Instruments:

RMS-4:	[2] (P 1201):	0dB
	[13] (EL 601):	0 dBm
	[4] (S 803):	70/140 MHz
	[7] (S 1301):	off
	[8] (S 902):	Sweep
	[9] (S 903):	70 MHz

	[17] (P 1305):	Right stop
	[20] (P 1302):	70 Hz
RME-4:	[29] (S 1601):	Input IF
	[31] (EL 701):	0 dBm (tracking)
	[36] (S 1401):	Tracking
	[37] (S 1402):	70 MHz
	[9] (S 2203): or [23] (S 2204):	Pushbutton "ΔP_I" pressed
	[2] (S 2201):	≈ (calibration lines on)

- With potentiometer [6] (P 309/ST-1), set calibration lines symmetrical to the horizontal center line
- With potentiometer P 312 on the Display Unit p.c.b. [698-A] adjust the calibration lines to coincide with the upper and lower graticule lines.

9.9. Adjustment of the Recorder-Calibration Line Distance

This adjustment can only be carried out on instruments, which are equipped with a recording attachment (BN 697/00.01).

Instrument Required:

1 X-Y recorder e.g. 7035B of Hewlett Packard

(The recorder connection cable is an accessory of the RME-4, when this is equipped with the recording attachment).

Measuring Setup: Back-to-back measurement RMS-4 - RME-4

Connection P_I [1] (Bu 1) and P_I input [27] (Bu 1)

Settings of the Instruments:

RMS-4:	[2] (P 1201):	0 dB
	[13] (EL 601):	0 dBm
	[4] (S 803):	70/140 MHz

	[7]	(S 1301):	off
	[8]	(S 902):	Sweep
	[9]	(S 903):	140 MHz
	[16]	(P 1501):	Right stop
	[17]	(P 1305):	5 MHz
	[18]	(S 801):	off
	[19]	(S 1501):	0.093 MHz or 0.083 MHz
	[20]	(1302):	70 Hz
RME-4:	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	140 MHz
	[2]	(S 2201):	≈ (calibration lines on)
	[9]	(S 2203):	Pushbutton "$\Delta\varphi,\Delta\tau$" depressed
	[10]	(S 2205):	100 ns
	[12]	(S 2602):	20 s
	[14]	(P 2203):	Center position
	[15]	(S 1503):	not pressed
	[23]	(S 2204):	Pushbutton "$\Delta U/U_o$" depressed
	[24]	(S 2202):	50%

- Raise plug-in card [697-AL...] or [697-CB...] by means of adaptor card [697-AT] , so that the components of the plug-in card become accessible
- With potentiometers [8] (P 2201) and [22] (P 2202) displace the $\Delta\varphi$, $\Delta\tau$- and $\Delta U/U_o$ test traces to the upper calibration lines in the CRT screen
- Start recording process and, with potentiometer P 2208, place

the $\Delta\varphi$, $\Delta\tau$ test trace on the upper calibration line of the X-Y recording chart

- In the case of the second image, place the $\Delta U/U_o$ test trace on the upper calibration line in the X-Y recording chart, using potentiometer P 2206
- Replace plug-in card [697 AL...] or [697-CB...] in the instrument and instead raise the plug-in card for the recording attachment [697-AJ]
- Switch over recording time to 2s with switch [12] (S 2602) at the RME-4
- With potentiometer [8] (P 2201), shift the $\Delta\varphi$, $\Delta\tau$ test trace to the lower calibration line in the CRT screen
- Start recording process and, with potentiometer P 2605, set the lower calibration line on the recorded $\Delta\varphi$, $\Delta\tau$ test trace

9.10. Adjust the IF Amplifier in the Tracking Path

An adjustment of the IF amplifier may be required after an exchange of components in the sub-assemblies (2) and (4), e.g. JC 201 or JC 401.

Instrument Required:

1	RF Millivoltmeter with VHF sensing head	e.g. 411A with 11023A of Hewlett Packa

Measuring Setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I output [1] (Bu 1) and P_I input [27] (Bu 1)

Settings of the Instruments:

RMS-4:	[2] (P 1201):	0dB
	[13] (EL 601):	0 dBm

	[4]	(S 803):	70/140 MHz
	[8]	(S 902):	Wideband
	[9]	(S 903):	70 MHz
	[17]	(P 1305):	Left stop
RME-4:	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	70 MHz

- Check the level at connection point (4) 68 on the board of the 140 MHz amplifier [697-0]
  value required: 265 mV $\pm$ 5 mV
- Check the level at connection point (7) 50 on the board of the input amplifier [697-V...]
  Value required: 120 mV $\pm$ 15 mV
- Provided that the level at connection point (4) 68 is correct and the level at connection point (7) 70 exceeds or is below the required tolerances, the value of the resistance R 211 must be increased or decreased by the same percentage.

9.11. Adjustment of 140 MHz IF Inside the Instrument

Instrument Required:

1 Frequency Counter (Up to 150 MHz) e.g. 5382 A Of Hewlett Packard

Measuring Set Up: Back-to-back measurment RMS-4 - RME-4
Connection between P_I-output [1] (Bu 1) and
P_I-input [27] (Bu 1)

Settings of the instruments:

RMS-4	[2] (P 1201):	0 dB
	[13] (EL 601):	0 dBm
	[4] (S 803):	70/140 MHz
	[9] (S 903):	70 MHz
	[17] (P 1305):	Left stop
RME-4	[29] (S 1601):	Input IF
	[31] (EL 701):	0 dBm (Tracking)
	[36] (S 1401):	Tracking
	[37] (S 1402):	70 MHz

- The 20 MHz IF is to be checked with the frequency counter connection point (4) 78 of the board of mixer II [697-W]

Value required: 20 MHz ± 20 kHz

- Now measure at connection point (4) 72 on the board of the 152 MHz low-pass filter [697-AS] and set the IF to 139.6 MHz ± 20 kHz with trimmer C 1206 (board [697-AH]).

9.12. Adjusting the Reference and Test Traces in the Δf and P_I Measurement

Measurement setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I-output [1] (Bu 1) and P_I-input [27] (Bu 1)

Settings of the instrument:

RMS-4	[2] (P 1201):	0 dB
	[13] (EL 601):	0 dBm
	[4] (S 803):	70/140 MHz

RMS-4 cont	8	(S 902):	Sweep
	9	(S 903):	70 MHz
	16	(P 1501):	500 kHz
	17	(P 1305):	Left stop
	19	(S 1501):	0.093 MHz or 0.083 MHz
RME-4	29	(S 1601):	Input IF
	31	(EL 701):	0 dBm (Tracking)
	36	(S 1401):	Tracking
	37	(S 1402):	70 MHz
	15	(S 1503):	Pushbutton "Δf, P_I" pressed

- Check on the CRT screen of the display unit whether the horizontal and vertical reference and test traces extend over the whole of the CRT screen
- If this is not the case, an adjustment must be made with potentiometer P 1501 on the plug-in card of switch X-Y 697-R .

Advice: In order to reach potentiometer P 1501, the plug-in cards to the right of plug-in card 697-R can be pulled out of the instrument. It is also possible to use the adaptor card 697-BK .

9.13. Adjusting the Deviation Measuring Recitifier (13)

Instruments required:

1 Digital voltmeter	e.g. 8600 A	of Fluke
1 Level sender	e.g. PS-14	of W&G
1 Oscilloscope	e.g. PM 3240	of PHilips

9.13.1. Preconduction Current and Symmetry

- With digital voltmeter, measure voltage between R 1318 and R 1319 on board 697-Q... and adjust to 0 V ±2 mV with potentiometer P 1301
- Measure voltage over R 1318 and adjust to 90 mV ± 0.5 mV with potentiometer P 1302

9.13.2. Linearity

- Short circuit pins 2 and 3 of IC 1301 on board 697-Q... and measure with oscilloscope at pin 6 of IC 1301
- Set potentiometer P 1303 so that the voltage jumps between its extreme values +U and -U or so that a value in between is shown
- Remove short circuit

9.13.3. Output Voltage

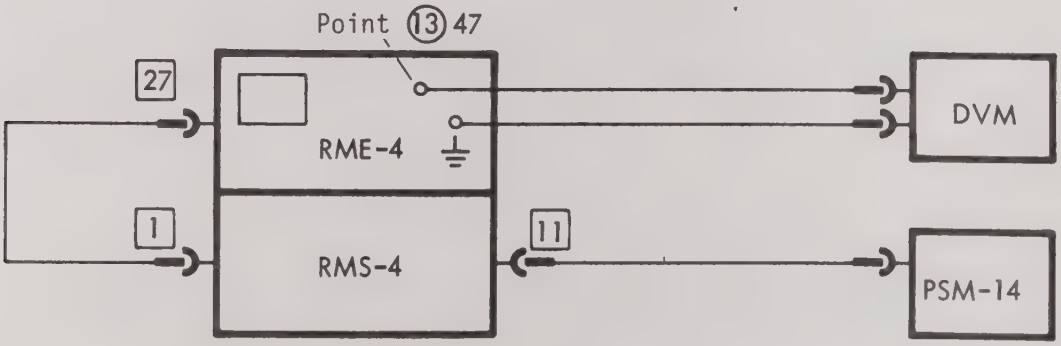


Fig. 9-5: Measuring setup for Section 9.13.3.

Settings of the instruments:

RMS-4	[2]	(P 1201):	0 dB
	[13]	(EL 601):	0 dBm
	[4]	(S 803):	70/140 MHz
	[8]	(S 902):	Wideband
	[9]	(S 903):	70 MHz
	[17]	(P 1305):	Left stop
RME-4	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (Tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	70 MHz
	[15]	(S 1503):	Pushbutton "Bessel" pressed

Level sender: f = 1.400 MHz

Send level ≈ -5 dBm

- On the CRT screen of the RME-4, produce Bessel zero by increasing the send level at the level sender ($\hat{=}$ Δf = 2.380 MHz)
- With potentiometer P 1305 on board [697-Q...], set the output voltage of the deviation measuring rectifier at connection point (13) 47 to -2380 mV ±3 mV
- With switch [8] (s 902), switch RMS-4 to the operating mode "sweep" and select test frequencies of 277 kHz or 250 kHz with switch [19] (S 1501)

- With potentiometer [16] (P 1501) on RMS-4, produce Bessel zero on the CRT screen of the RME-4 ($\hat{=}$ Δf = 472.39 kHz or 425.15 kHz)

- With potentiometer P 1308, set an output voltage at point (13) 47 to be -2361 mV ± 3 mV at 277 kHz or -2126 mV ± 3 mV at 250 kHz.
- If necessary, carry out the settings alternately.
- Release pushbutton [15] (S 1503) "Bessel" at the RME-4 and instead press pushbutton "Δf, PI"
- Bring CAL potentiometer [13] (P 1304) into the center position and, with potentiometer P 1305, set the deviation indication on the Bessel marker ∇ .

9.14. Adjustment of the Main Regulating Circuit (10)

Instrument required:

1 Frequency counter (up to 25 MHz)	e.g. FZ-4	of W&G
1 Digital voltmeter	e.g. 8600 A	of Fluke

Measurement setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I-output [1] (Bu 1) and P_I-input [27] (Bu 1)

Settings of the instruments:

RMS-4	[2] (P 1201):	0 dB
	[13] (EL 601):	0 dBm
	[4] (S 803):	70/140 MHz
	[8] (S 902):	Sweep
	[9] (S 903):	70 MHz
	[17] (P 1305):	Left stop
RME-4	[29] (S 1601):	Input IF
	[31] (EL 701):	0 dBm (Tracking)
	[36] (S 1401):	Tracking
	[37] (S 1402):	70 MHz

9.14.1. Operating Voltage for JC 1001

- Measure voltage at TP 1001 on board 697-E... with digital voltmeter and set to +5 V ± 20 mV with potentiometer P 1001

9.14.2. IF Setting

- Open bridge (10) a-b on the board of the main regulating circuit 697-E...
- Connect frequency counter to connection point (2) 105 of the board of the all-pass filter 697-AO and set the IF to 20 MHz ±100 kHz with potentiometer P 1003
- After the adjustment close bridge (10) a-b once again

9.15. Setting the Input Amplifier (7)

Instruments required:

1 Digital voltmeter	e.g. 8600 A	of Fluke
1 Return loss measuring bridge	e.g. RFZ-4	of W&G
1 Calibration level meter with sensing head	e.g. EPM-1 with TK-10	of W&G
1 Oscilloscope	e.g. PM 3240	of Philips

9.15.1. Operating Points in the Input Regulating Amplifier

- With digital voltmeter at emitter from T 702, set voltage of 8.5 V ±50 mV on board 697-V... with potentiometer P 702
- Measure collector emitter voltage from T 703

Value required: 4 V ±0.5 V

- If the required value is not maintained, resistance R 712 is to be altered appropriately

- Subsequently, the setting of potentiometer P 702 is to be checked and, if necessary, corrected.

9.15.2. Return Loss at IF Input P_I

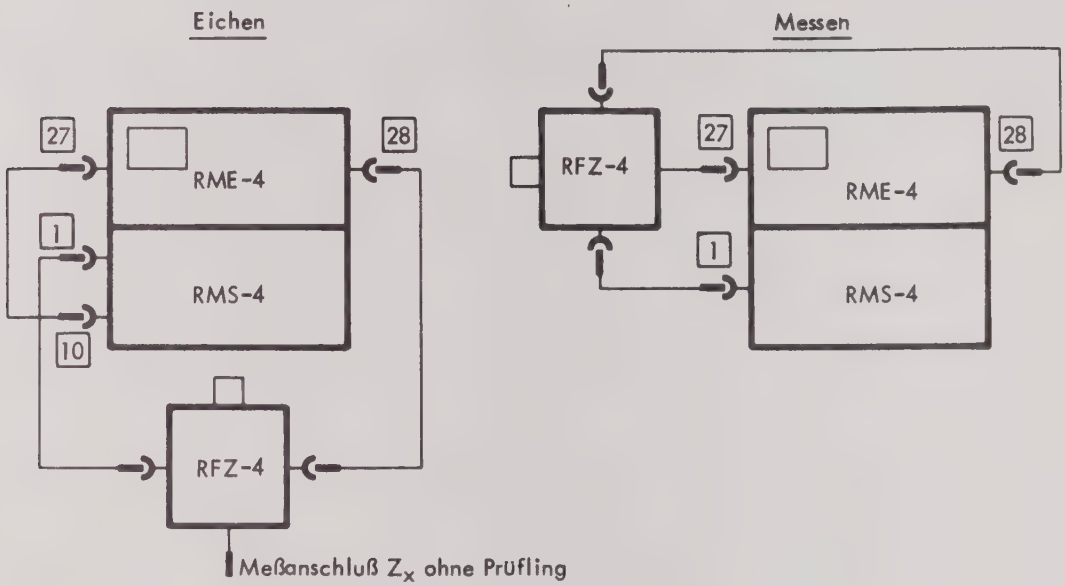


Fig. 9-6: Measurement setup for Section 9.15.2.

Key for Figure 9-6:

Eichen	=	Calibration
Messen	=	Measurement
Messanschluss Z_x ohne Prüfling	=	Test connection Z_x without component to be tested

Settings of the instruments:

RMS-4 [2] (P 1201): 0 dB

[13] (EL 601): -10 dBm

RMS-4 cont.	[4] (S 803):	70/140 MHz
	[7] (S 1301):	off
	[8] (S 902):	Sweep
	[9] (S 903):	140 MHz
	[17] (P 1305):	25 MHz
	[18] (S 801):	2 $\hat{\Delta F}$
RME-4	[29] (S 1601):	Input IF
	[31] (EL 701):	0 dBm (Tracking)
	[36] (S 1401):	Tracking
	[37] (S 1402):	140 MHz
	[9] (S 2203):	Pushbutton "ΔP_{II}" pressed
	[14] (P 2203):	Right stop
	[15] (S 1503):	Not pressed

Calibration:

- Equip a measuring setup for calibration, as shown in Figure 9-6
- With potentiometer [8] (P 2201) set the a_r test trace on the 0 dB graticule line

Measurement and adjustment:

- Equip a measuring setup for measuring as shown in Figure 9-6
- Change-over [31] (EL 701) to "-10 dBm"
- Required value of the return loss in the range of 140 MHz $\pm$ 50 MHz
  $a_r \geq 26$ dB
- The adjustment is carried out on board [697-V...] by changing the strap L 703 and by changing the distance between turns of L 702.

9.15.3. Operating Point of the Detector Amplifier (omitted for series B and C)

- with digital voltmeter, measure at collector of transistor T 2 (thin-film circuit DSS-703) on board 697-V...

Value required: 4 V ±0.5 V

- If necessary, adjust by changing resistance R 735

9.15.4. Preconduction Current and Symmetry of the Display Rectifier

- With the digital voltmeter, measure voltage between pin 2 (≙ TP 701) and pin 3 of IC 702 on board 697-V... and adjust to 0 V ± 2 mV with potentiometer P 703
- Adjust voltage at TP 701 to 150 mV ±2 mV with potentiometer P 704
- Repeat first measurement and, if necessary, correct

9.15.5. Linearity of the Display Rectifier

- Short circuit pin 2 and pin 3 of IC 702 on board 697-V... and measure at pin 6 of IC 702 with oscilloscope
- Set potentiometer P 705 so that the voltage jumps between its extreme values +U and -U or indicates a value in between
- Remove short circuit

9.15.6. Output Voltage of the Display Rectifier

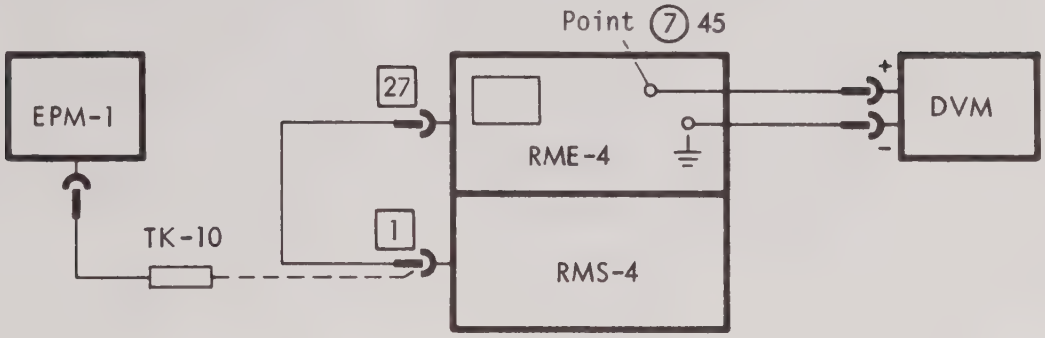


Fig. 9-7: Measuring setup for Section 9.15.6.

Settings of the instrument:

RMS-4	[2]	(P 1201):	0 dB
	[13]	(EL 601):	0 dBm
	[4]	(S 803):	70/140 MHz
	[8]	(S 902):	Sweep
	[9]	(S 903):	70 MHz
	[17]	(P 1305):	Left side
RME-4	[29]	(S 1601):	Input IF
	[31]	(EL 701):	0 dBm (Tracking)
	[36]	(S 1401):	Tracking
	[37]	(S 1402):	70 MHz

EPM-1 Test range ±0.2 dBm, TK-10 calibrated with 0 dBm, R_i = 75 Ω

- With the milliwatt power meter, set the IF send level of the [RMS-4] at socket [1] (Bu 1) to 0 dBm ±0.02 dB

- Connect P_I sockets of RMS-4 and RME-4
- With potentiometer P 706 on board [697-V...], set the output DC voltage at connection point (7) 45 to -4000 mV
- With swicht [36] (S 1401), switch RME-4 to the operating mode "wide-band" and bring switch [31] (EL 701) in the position of 0 dBm (wide-band). With potentiometer P 707, set the output voltage at connection point (7) 45 to -4000 mV.

9.15.7. Frequency Response ΔP_I

Measuring setup: Back-to-back measurement RMS-4 - RME-4
Connection between P_I-output [1] (Bu 1) and P_I-input [27] (Bu 1)

Advice: The short-circuit connection should be established with the short 75 Ω cable supplied.

Settings of the instruments:

RMS-4	[2] (P 1201):	-5 dBm
	[13] (EL 601):	+10 dBm
	[4] (S 803):	70/140 MHz
	[7] (S 1301):	off
	[8] (S 902):	Sweep
	[9] (S 903):	70 MHz
	[16] (P 1501):	Left stop
	[17] (P 1305):	25 MHz
	[18] (S 801):	2 $\hat{\Delta F}$
	[20] (S 1302):	70 Hz

RME-4

29	(S 1601):	Input IF
31	(EL 701):	+10 dBm (Tracking)
36	(S 1401):	Tracking
37	(S 1402):	70 MHz
14	(P 2203):	Right stop
9	(S 2203):	Pushbutton "ΔP_I" and "ΔP_{II}" depressed simultaneously ($\hat{=}$ high ΔP_I sensitivity)

Advice: For the frequency response adjustment, the shield cover on the printed circuit of the input amplifier (7) board 697-V... must be closed.

- Read off frequency response ΔP_I on the CRT screen on the display unit

Value required: max. ±0.05 dB

- The adjustment for the range 70 MHz ±25 MHz is carried out with the coil L 704 on board 697-V...
- With switch 9 (S 903) or 37 (S 1402), switch RMS-4 and RME-4 over to the IF of 140 MHz
- For the range 140 MHz ±50 MHz the adjustment is made with trimmer C 726 to the required value of max. ±0.1 dB

Note: After removal of the left side wall, C 726 is accessible through a borehole in the circuit tub.

9.16. Adjustment of the Matching Amplifier (5)

Test instruments required:

1 Digital voltmeter e.g. 8600 A of Fluke

1 Selective level meter	e.g. SPM-14	of W&G
1 Function generator	e.g. Model 180	of Wavetek
1 Oscilloscope	e.g. PM 3240	of Philips

9.16.1. Operating Point of Transistor T 503

- With digital voltmeter, measure voltage over R 507, that is, at connection point (5) 11 on board [697-T] and connection point (5) 1 on board [697-AP]
- Dimension R 505 on the a-b terminals so that the digital voltmeter shows a voltage of 127 mV ±10 mV

Advice: The adjustment should be made only after a 1-hour warming-up time with shield cover closed on board [697-T]

Whenever T 503 is exchanged, the distortions, caused by the matching amplifier, must be checked. For this purpose, the amplifier is to be opened at connection point (5) 17 and fed from the direction of the RMS-4 with a BB signal over an appropriatly prepared cable.

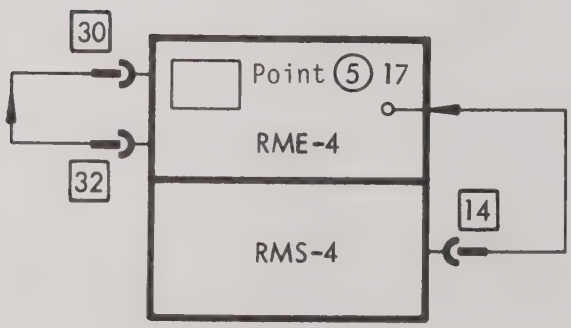


Fig. 9-8 Measuring setup for checking the matching amplifier distortions

Settings of the instrument:

RMS-4	[6]	(P 1303):	±18 MHz
	[7]	(S 1301):	on
	[15]	(S 1601):	Not pressed
	[16]	(P 1501):	200 mV
	[17]	(P 1305):	0.8 V
	[20]	(S 1302):	70 Hz
RME-4	[29]	(S 1601):	Input BB (Distortion)
	[34]	(S 1602):	U_x from BB
	[9]	(S 2203):	Pushbutton "$\Delta\varphi, \Delta\tau$" depressed
	[10]	(S 2205):	0.5% rad
	[23]	(S 2204):	Pushbutton "$\Delta U/U_o$" depressed
	[24]	(S 2202):	0.5%
	[11]	(S 601) :	6 kHz / 0 MHz

- Measure distortions at all test frequencies; the following values must be maintained

  $\Delta\varphi, \Delta\tau \leq 0.5\%$ rad, $\Delta U/U_o \leq 0.5\%$

  - If these values are not maintained, T 503 must be exchanged

  Note: A tilted position of the $\Delta\varphi$ distortion can be corrected with C 529 at the frequency of 8.2 MHz.

9.16.2. Output DC Voltage

- With the digital voltmeter, measure DC voltage at the BB output [32] (Bu 501) and adjust to 0 V ±0.1 V with potentiometer P 501 on board [697-T]

9.16.3. Demodulation Transconductance

Advice: The adjustment of the demodulation transconductance is necessary only after an exchange of the demodulator (27) sub-assembly

Measurement setup: Back-to-back measurement RMS-4 - RME-4
Connection between P_I-output [1] (Bu 1) and P_I-input [27] (Bu 1)

Settings of the instruments:

RMS-4	[2] (P 1201):	0 dB
	[13] (EL 601):	0 dBm
	[4] (S 803):	70/140 MHz
	[8] (S 902):	Sweep
	[9] (S 903):	70 MHz
	[17] (P 1305):	Left stop
	[19] (S 1501):	0.277 MHz or 0.250 MHz
RME-4	[29] (S 1601):	Input IF
	[31] (EL 701):	0 dBm (Tracking)
	[36] (S 1401):	Tracking
	[37] (S 1402):	70 MHz
	[15] (S 1503):	Pushbutton "Bessel" depressed

- At RMS-4, set the test deviation with potentiometer [16] (P 1501) so that the carrier disappears on the CRT screen of the visual unit (Bessel zero)
- Measure output level at socket [32] (Bu 501) with the selective level meter

Value required: -21.29 dBm ± 0.25 dB for f_M = 277 kHz
-22.20 dBm ± 0.25 dB for f_M = 250 kHz

- If necessary, the value may be corrected by changing R 551 on board [697-T]

9.16.4. Tilt in the Case of a 50 Hz Square Modulation

Advice: The adjustment of the tilt in the case of a 50 Hz square modulation is necessary only after the demodulator sub-assembly (27) or the capacitors C 507, C 514, C 515 and C 516 are exchanged!

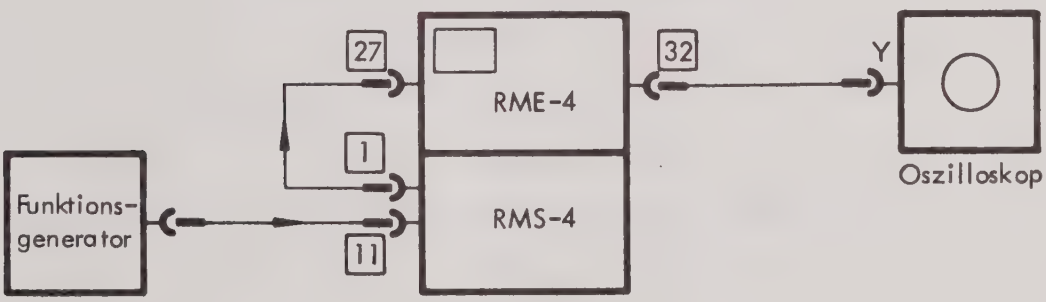


Fig. 9-9 Measuring setup for Section 9.16.4.

Key for Figure 9-9:

Funktionsgenerator	=	Waveform generator
Oszilloskop	=	Oscilloscope

Settings of the instruments:

RMS-4	[2] (P 1201):	0 dB
	[13] (EL 601):	0 dBm

	[4] (S 803):	70/140 MHz
	[8] (S 902):	Wideband
	[9] (S 903):	70 MHz
RME-4	[29] (S 1601):	Input IF
	[31] (EL 701):	0 dBm (Wideband)
	[36] (S 1401):	Wideband
	[37] (S 1402):	70 MHz

Waveform generator: f = 50 Hz, signal shaped: square

- Set voltage at waveform generator so that 500 mV_{pp} is measured with the oscilloscope at the BB output [32] (Bu 501)
- Expand test result on the oscilloscope so that the tilt of the square signal is easily readable

Value required: < 1% $\hat{=}$ 5 mV (Caution! In the case of overshoot distortion, it is possible to falsify the test result)

- If the value is not complied with, an adjustment is possible by changing C 514

9.17. Adjustment of the Level Regulation Circuit After an Exchange of the Demodulator (27)

Advice: The adjustment of the level regulating circuit is required only after the exchange of the demodulator sub-assembly (27) !

In addition, after a demodulator is exchanged, the slope and tilt in the case of 50 Hz square-wave modulation should be checked and, if necessary, adjusted (see Section 9.16.)

Test instrument required:

1 RF Millivoltmeter with VHF sensing head	e.g. 411 A with 11023 A	of Hewlett Packard

Test setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I-output [1] (Bu 1) and P_I-input [27] (Bu 1)

Settings of the instruments:

RMS-4	[2] (P 1201):	0 dB
	[13] (EL 701):	0 dBm
	[4] (S 803):	70/140 MHz
	[8] (S 902):	Sweep
	[9] (S 903):	70 MHz
	[17] (P 1305):	Left stop
RME-4	[29] (S 1601):	Input IF
	[31] (EL 701):	0 dBm (Tracking)
	[36] (S 1401):	Tracking
	[37] (S 1402):	70 MHz

- With the RF millivoltmeter at the output of the 140 MHz amplifier, measure connection point (4)68 (board [697-0]) and adjust the voltage to 265 mV ± 5 mV with potentiometer P 1612

9.18. Adjustment of the U_x Generation (16)

Advice: The adjustment is required when the phase position of the deflection voltage U_x is altered in the tracking mode for different sweep widths

Test instruments required:

1 Frequency counter	e.g. FZ-4	of W&G
1 Distortion Analyzer	e.g. SPM-11/PSE-11	of W&G
1 Oscilloscope with a 10:1 sensing head	e.g. PM 3240 with PM 9350	of Philips

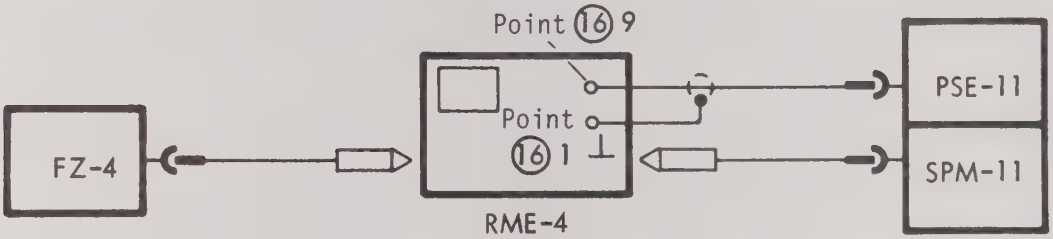


Fig. 9-10: Measuring setup for Section 9.18.

Settings of the instruments:

RME-4	[29] (S 1601): Input IF
PSE-11	f = 70 Hz, send level -30 dB

- Unsolder lead at connection point (16) 9 on board [697-G] and connect level sender as shown in Figure 9-10
- Measure with level meter at TP 1601 and make a k_2 minimum adjustment with potentiometer P 1601
- Measure with the level meter at connection point (16) 4 and make a k_2 minimum adjustment of the deflection frequency with potentiometer P 1602 and set the output voltage to + 13.2 dB with potentiometer P 1603
- At RME-4, depress the pushbutton [15] (S 1503) "Bessel"

- Measure with frequency counter at connection point (16) 4 and set 18 Hz with potentiometer P 1607
- Now setup test equipment as shown in Figure 9-11

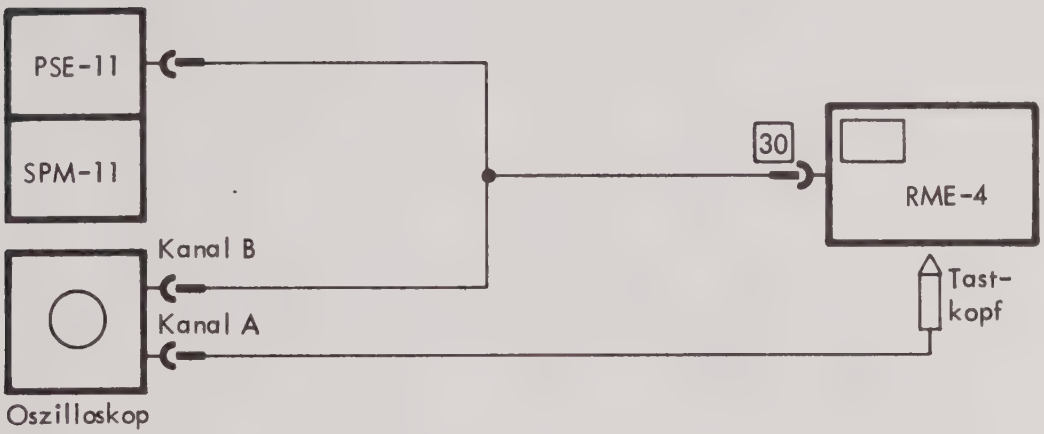


Fig. 9-11

Key for Figure 9-11:

Kanal	=	Channel
Tastkopf	=	Sensing Head
Oszilloskop	=	Oscilloscope

Settings of the instruments:

RME-4	29 (S 1601):	Input IF (Distortion)
	34 (S 1602):	U_x from BB
PSE-11	f = 110 Hz, send level -25 dB	
Oscilloscope	Channel A: 0.5 V/cm	
	Channel B: 0.2 V/cm	

Time base: 2 ms/cm

Operating mode: Chopper operation, trigger internal from Channel B

- Measure with sensing head at R 1688 on board 697-G
- Set potentiometer P 1608 so that a negative slope can be displaced by more than the duration of one period of the sinusoidal signal (about 5 cm), when potentiometer 35 (P 1609) is turned from stop to stop
- Set a frequency of 18 Hz at the level sender and a time base of 10 ms/cm at the oscilloscope
- Check whether the negative slope of the sinusoidal signal can be displaced by more than the duration of one period (about 6 cm).

9.19. Adjustment Instructions for the Display Unit ST-1

The display unit must be adjusted after the installation of a new picture tube.

Advice: Some of the boards of the display unit carry dangerous voltages. Use only insulated tools for the adjustment work.

9.19.1. Visual Quantities

In order to adjust the visual quantities of the display unit, the IF level and r.m.s. frequency deviation method of representation is to be used, in which a horizontal and vertical pair of traces is formed

Test setup: Back-to-back measurement RMS-4 - RME-4

Connection between P_I-output [1] (Bu 1) and P_I-input [27] (Bu 1)

Settings of the instruments:

RMS-4	[2] (P 1201):	0 dB
	[13] (EL 601):	0 dBm
	[4] (S 803):	70/140 MHz
	[8] (S 902):	Sweep
	[9] (S 903):	70 MHz
	[16] (P 1501):	500 kHz
	[17] (P 1305):	Left stop
	[19] (S 1501):	0.093 MHz or 0.083 MHz
RME-4	[29] (S 1601):	Input IF
	[31] (EL 701):	0 dBm (Tracking)
	[36] (S 1401):	Tracking
	[37] (S 1401):	70 MHz
	[15] (S 1503):	Pushbutton "Δf, P_I" depressed

9.19.1.1. Beam Position

- With potentiometer [2] (P 1201) on the RMS-4, shift the test trace for the IF level to the center of the CRT screen
- With potentiometer P 203 on board [698-C], turn test trace until it is parallel to the graticule line

9.19.1.2. Correcting Pincushion or Barrel Distortion (Geometry)

- Potentiomer [2] (P 1201) on the RMS-4 again in the 0 dB

position; other settings as in Section 9.20.1.

- Set the horizontal pair of lines to full vertical gain (≙ 75 mm) with potentiometer P 312 on board 698-A; with potentiometer 6 (P 309/ST-1) set the lines on the upper and lower graticule lines
- Set the vertical pair of lines to full horizontal gain (≙ 83 mm) with potentiometer P 306 on board 698-A; with potentiometer 5 (P 308)/ST-1), set the lines on the left and right graticule lines
- With potentiometer P 201 on board 698-C, the pincushion or barrel distortions are to be corrected optimally; if necessary, average between the distortions in horizontal and vertical directions
- With potentiometers P 314 and P 306, again bring the line separations to full vertical or horizontal gain
- After the distortion has been corrected, the lines should not deviate anywhere from the graticule boundary by more than 2% of the line separation.

9.19.1.3. Astigmatism

- The lower horizontal and the left vertical lines remain on the graticule boundary
- Shift the upper horizontal line with potentiometer 2 (P 1201) on the RMS-4 to the center of the CRT screen
- Shift the right vertical line with potentiometer 16 (P 1501) on the RMS-4 to the center of the image
- With potentiometer 3 (P 206/ST-1), set an average beam intensity

- Focus vertical lines approximately equally with potentiometer "focus" [4] (P 403/ST-1) on the RME-4
- Match the focus of the horizontal lines with potentiometer P 202 on board [698-C] to that of the vertical lines
- Repeat the process alternately until all lines have the same beam width

9.19.1.4. Brightness

- Set the line pairs as in Section 9.20.1.3.

Advice: The adjustment, described below, should be made only after a warming-up period of about 30 minutes

- Turn potentiometers P 204 and P 205 on board [698-C] to the middle position and potentiometer "intensity" [3] (P 206/ST-1) to the right stop
- Shift potentiometer P 204 until the lines are about one small graticule division (about 1.5 mm) wide
- Turn potentiometer [3] (P 206/St-1) to the left stop and adjust the bridhtness with potentiometer P 205 until the lines are no longer visible
- Repeat the alignment of P 204 and P 205.

9.19.2. Image Linearity

In order to adjust the image linearity, the X and Y inputs to the display unit are opened and a calibration voltage is applied.

At certain DC voltages, defined excursions in the X and Y directions must arise as a verticle or a horizontal beam on the CRT screen. The linearization, that is, the adjustment to the expected value, is carried out on the outermost graticule

lines. The necessary corrective adjusting elements and the diode configuration in Table 9-4. Linearity deviations up to about ± 1% at full deflection can be elimenated with the "weak" correction. In the case of greater linearity deviations, the "weak" and "strong" corrections are to be combined. An optimum linearity setting can be achieved by correcting repeatedly with the potentiometers for "weak" and "strong".

Advoid parallax errors when making the linearity adjustment.

9.19.2.1. X Linearity

- On the reverse side of the display unit, remove short circuit male connectors between X input and output at sockets [54] and [55].
- Connect calibrating voltage at socket [55] X⊙. See Figure 9-12 for the production of the calibration voltage.
- Place connection point (2) 15 on board [698-C] on 0 V (LOW).

Kalibrierspannung	Korrektur mit	Strahlposition auf der Rasterscheibe	
0,000 V	5 (P 308)	250 kHz	
+1,500 V ±2‰	P 306	400 kHz	
+2,500 V ±2‰	-	500 kHz	Abweichung feststellen
-2,500 V ±2‰	-	0 kHz	Abweichung feststellen

Table 9-2: Determination of the linearity deviations in the X direction

Key for Table 9-2:

Kalibrierspannung	=	Calibration voltage
Korrektur mit	=	Correction width
Strahlposition auf dem Bildschirm	=	Beam position on the CRT screen
Abweichung feststellen	=	Determine deviation

- Adjust deviations determined with the help of Table 9-4, as described in Section 9.19.2.
- In the case of calibration voltages ±1 V, ±1.5 V, ±2 V and ±2.5 V, recheck linearity

Suggestions for making the measurements:

A calibration voltage of the required accuracy can be produced with the help of a voltage divider. A helical 10-turn potentiometer can be used as the voltage divider. The voltage settings are checked with the help of a digital voltmeter of appropriate accuracy.

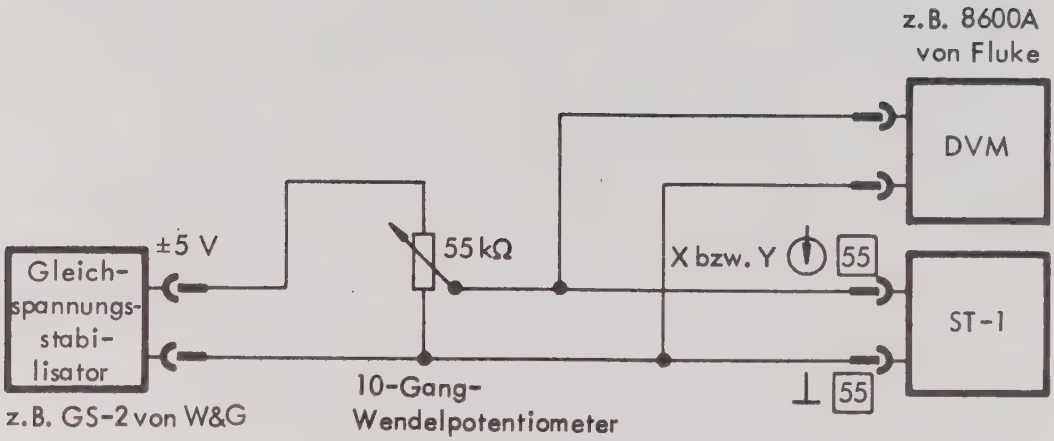


Fig. 9-12: Production of the calibration voltage

Key for Figure 9-12:

Gleichspannungsstabilisator	=	DC voltage stabilizer
z.B. GS-2 von W&G	=	e.g. GS-2 of W&G
10-Gangwendelpotentiometer	=	Helical 10-turn potentiomete
bzw.	=	or
z.B. 8600A von Fluke	=	e.g. 8600A of Fluke

9.19.2.2. Y linearity

- On the reverse side of the display unit, remove short circuit male connector between Y output and input at the sockets [54] and [55]
- Connect a calibration voltage to socket [55] Y ⏚ .

See Fig. 9-12 for the production of the calibration voltage.

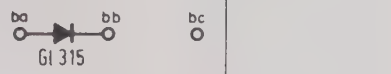
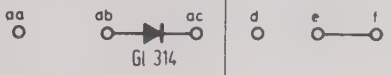
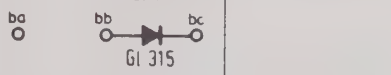
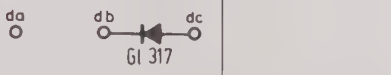
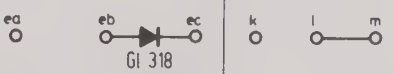
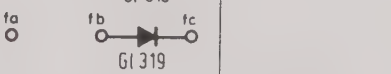
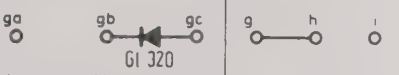
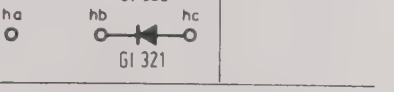
Kalibrierspannung	Korrektur mit	Strahlposition auf der Rasterscheibe	
0,000 V	6 (P 309)	- 5 dB	
+1,500 V ±2‰	P 312	- 2 dB	
+2,500 V ±2‰	-	0 dB	Abweichung feststellen
-2,500 V ±2‰	-	-10 dB	Abweichung feststellen

Table 9-3: Determination of the linearity deviations in the Y direction

Key for Table 9-3:

Kalibrierspannung	=	Calibration voltage
Korrektur mit	=	Correction width
Strahlposition auf dem Bildschirm	=	Beam position on the CRT screen
Abweichung feststellen	=	Determine deviation

- Adjust the deviations determined with the help of Table 9-4, as described in Section 9.19.2.
- In the case of calibration voltages of ±1 V, ±1.5 V, ±2 V and ±2.5 V, recheck linearity
- Check adjustment according to Section 9.8

Bildteil	Linearitäts-Abweichung	Korrektur mit	Wirkung	Pot.-stellung vor Korr.	Bestückung
rechts	progressiv	P 307	schwach	RA	
		P 305	stark	RA	
	degressiv	P 307	schwach	LA	
		P 305	stark	LA	
links	progressiv	P 304	schwach	LA	
		P 302	stark	LA	
	degressiv	P 304	schwach	RA	
		P 302	stark	RA	
oben	progressiv	P 310	schwach	RA	
		P 311	stark	RA	
	degressiv	P 310	schwach	LA	
		P 311	stark	LA	
unten	progressiv	P 313	schwach	LA	
		P 314	stark	LA	
	degressiv	P 313	schwach	RA	
		P 314	stark	RA	

Alle Dioden BAY 73

RA: rechter Anschlag
LA: linker Anschlag

Table 9-4: Linearity Correction

Key for Table 9-4:

Bildteil	=	Section of image
Linearitäts-Abweichung	=	Linearity deviation
Korrektur mit	=	Correction with
Wirkung	=	Effect
Potstellung vor Korr	=	Potentiometer position before correction
Bestuckung	=	Equipment
rechts	=	Right
links	=	Left
oben	=	Top
unten	=	Bottom
progressiv	=	Progressive
degressiv	=	Degressive
schwach	=	Weak
stark	=	Strong
Alle Dioden BAY 73	=	All BAY 73
RA	=	Right stop
LA	=	Left stop

9.19.3. Adjustment of the Gain Limitation and the Constant Current For the X and Y Deflection Amplifier

Test Instruments Required:

1 Digital ammeter	e.g. 8000 A	von Fluke
1 Digital Voltmeter	e.g. 8000 A	von Fluke

Note: Board [698-A] in the display unit carries dangerous voltages at several sites. The constant current should be adjusted only with insulated tools. Before any soldering work is carried out, the instrument must be switched off.

- Test set up and adjustments as in Section 9.19.1.
- Remove bridge n-o on board [698-A] in the display unit and insert digitalammeter between the soldering terminals.
- For the later adjustment of the gain limitation, set the constant current at 10 mA with potentiometer P 317
- Connect digital voltmeter via decoupling resistors of 47kΩ to the outputs of the X amplifier, connection point (3) 3 and connection point (3) 4 or to the outputs of the Y amplifier, connection point (3) 1 and connection (3) 2 on board [698-A] and adjust the voltage difference with potentiometer [5] (P 308/ST-1) or [6] (P309/ST-1) to 0 V $\pm$0.5 V.
- Apply DC voltages to the X and Y input of the display unit as indicated in Table 9-5 and adjust gain limitation also as described in Table 9-5; the DC voltages are supplied as described in Section 9.19.2.1. or 9.19.2.2.

Eingangs-spannung X	Eingangs-spannung Y	Ausgangsspannung Pkt. ③1	Pkt. ③2	Pkt. ③3	Pkt. ③4	Abgleich mit Potentio-meter
+12 V	-	-	-	-	252.0 ±0.5 V	P 303
-12 V	-	-	-	252.0 ±0.5 V	-	P 301
-	+12 V	-	193.5 ±0.5 V	-	-	P 315
-	-12 V	193.5 ±0.5 V	-	-	-	P 316

Table 9-5: Adjustment of the Gain Limitation

Key For Table 9-5:

Eingangsspannung	=	input voltage
Ausgangsspannung	=	output voltage
Abgleich mit Potentio-meter	=	adjustment with potentiometer

- with an input voltage of 0 V, adjust constant current with potentiometer P 317 to 9.2 mA $\pm$0.1 mA
- after about 5 minutes, check adjustment and, if necessary, adjust
- solder bridge n-o back in place, replace short-circuit male connector

9.19.4. Adjustment at the High-Voltage Part

Test instruments required:

1 Digital Voltameter	e.g. 8600 A	von Fluke
1 High-voltage sensing head	e.g. 80 K-40	von Fluke

Note: Board [698-B] carries dangerous voltages at several sites. The adjustment work should be carried out only with insulated tools. For any soldering, switch off the instrument.

9.19.4.1. Offset voltage from JC 402

The adjustment is required only after replacement of IC 402

- Remove bridges a-b and c-d on board [698-B] and connect connection point b to the chassis
- Connect digital voltmeter to connection point c (output from IC 402) and adjust the offset voltage with potentiometer P 402 to 0 V ± 20 mV
- subsequently solder bridges back in place.

9.19.4.2. Oscillator Frequency

The adjustment is required only after the replacement of Ü 401, L 401, C 412 or C 413.

- Adjust current consumption from +12 V, connection point ④ 26, to a minimum with L 401
- If the minimum of the current consumption does not fall within the adjustment range of L 401, the adjustment range must be shifted by altering the shunt capacitance C 413.

9.19.4.3. High Voltage

- Measure high voltage at connection point ④ 14 with a high-voltage sensing head and digital voltmeter and adjust with potentiometer P 401 to -1250 V $\pm$10 V.

9.20 INSTRUCTIONS FOR ADJUSTING THE BF LEVEL METER

Note: To carry out the measurements and adjustments described below (apart from Section 9.20.1.), it is recommended that the plug-in card [697-CJ] be raised using the adapter card [697-AT] to make the components and measuring points easily accessible.

9.20.1 ADJUSTMENT OF THE CALIBRATED OSCILLATOR

Measuring instruments required:

1 Milliwatt Power Meter with sensing head 75 Ω	e.g. EPM-1 with TK-10	supplied by W&G
1 Level Generator	e.g. PS-14	supplied by W&G
1 calibrated attenuator	e.g. D 120	supplied by Siemens

Setting the instruments:

EPM-1: Measuring range 0 dBm ±0.2 dB
PS-14: f = 100 kHz, level = 0 dBm
Calibrated
attenuator: Attenuation = 30.00 dB
RME-4: [29] (S 1601): BF level P_{BF}
[42] (S 3401): Middle setting, P_{BF}

- Using the calibrated level meter, set the output level of the Level Generator to exactly 0 dBm.
- Connect the Level Generator via the calibrated attenuator to socket [30] (socket 1901) of the RME-4
- Set the BF level indication to -30.00 dBm using [41] (P 3203)
- Turn switch [42] (S 3401) to the right to position "Cal." and readjust BF level indication to -30.00 dBm using P 3401.

9.20.2 ADJUSTMENT OF THE OPERATING POINT OF TRANSISTOR T 3211

Note: This adjustment is only necessary if transistor T 3210 or T 3211
3210 or T 3211 have been changed.

Measuring instrument required:

1 digital multimeter e.g. 8000 A supplied by Fluke

- Solder in a 100 kΩ potentiometer for resistor R 3277 and set this at approximately 50 kΩ.

- Measure voltage at resistor R 3281 using the digital voltmeter and set potentiometer P 3201 to 2.5 V.
- Measure voltage at the collector of transistor T 3211 with respect to earth and adjust to 6 V using the 100 kΩ potentiometer.
- Measure set resistance value of the potentiometer and solder in an appropriate film resistor (±5%) for R 3277.
- As a check, measure voltage at resistor R 3281 again and, if necessary, readjust using potentiometer P 3201

  Requisite value: 2.5 V ±0.1 V
- Check voltage at the collector of transistor T 3211

  Requisite value: 6 V ±0.5 V

9.20.3 ADJUSTMENT OF THE LEVEL INDICATION (DC voltage processing circuit)

Measuring instruments required:

1 Milliwatt Power Meter with Test Probe 75 Ω	e.g. EPM-1 with TK-10	supplied by W&G
1 T-piece 75 Ω	e.g. BN 595/1	supplied by W&G
1 Level Generator	e.g. PS-14	supplied by W&G
1 calibrated attenuator	e.g. D 120	supplied by Siemens
1 digital voltmeter	e.g. 8600 A	supplied by Fluke

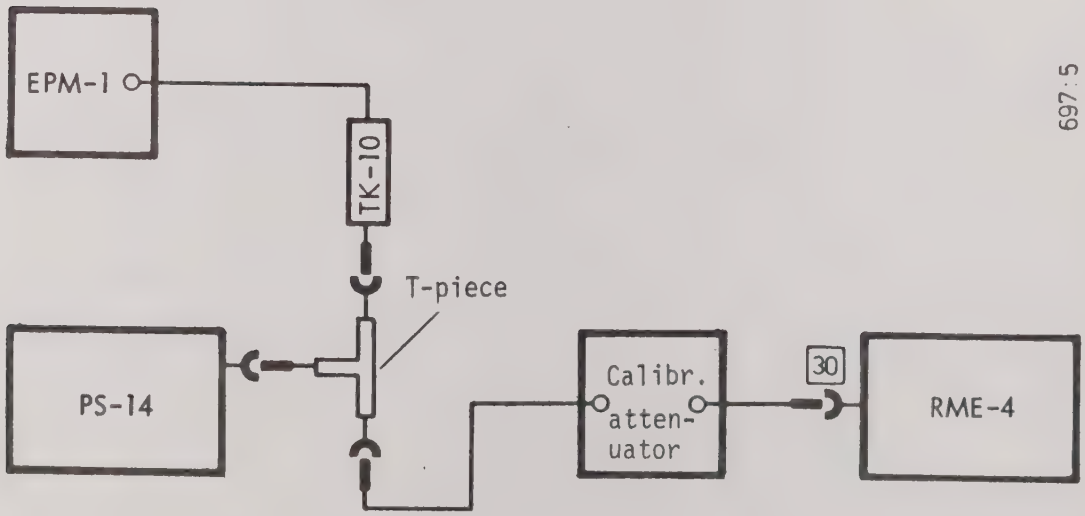


Fig. 9-13 Measuring set-up for Section 9.20.3.

Settings on the instruments:

EPM-1: Measuring range 0 dBm ±0.2 dB

PS-14: f = 100 kHz, level +6 dBm

Calibrated attenuator: Attenuation = 50 dB

RME-4: [29] (S 1601): BF level P_{BF}

[42] (S 3401): Left-hand setting, P_{BF}

- Measure the voltage at test point TP 3402 on the indicator circuit [697-CK] (behind front panel) using digital voltmeter and set to 1.000 V ±1 mV using potentiometer P 3403.
- Adjust Cal. potentiometer [41] (P 3203) to middle setting.
- Adjust output level of the PS-14 so that the calibrated EPM-1 indicates 0 dBm. Connect the digital voltmeter to test point TP 3202 on the plug-in card [697-CJ]. Using P 3204, set voltage to 0 V ± 20 mV.
- Switch over measuring range on the EPM-1 to +1 dBm and adjust output-level of the PS-14 to +1 dBm. Voltage at TP 3202 must now be -5 V ±30 mV. In case of deviation, readjust the gain using P 3202.
- Repeat adjustment for 0 dBm and +1 dBm until the requisite values of 0 V ±20 mV and -5 V ±30 mV have been reached.
- Readjust output level to 0 dBm and set the BF Level Meter indication to -50.00 dBm using P 3204.
- Adjust output level to +1 dBm and adjust the BF Level Meter indication to -49.00 dBm using P 3205.

9.20.4 DIVIDER ADJUSTMENT

Measuring instruments required:

1 Level Meter	e.g. PS-14	supplied by W&G
1 calibrated attenuator	e.g. D 120	supplied be Siemens
1 digital voltmeter	e.g. 8600 A	supplied by Fluke

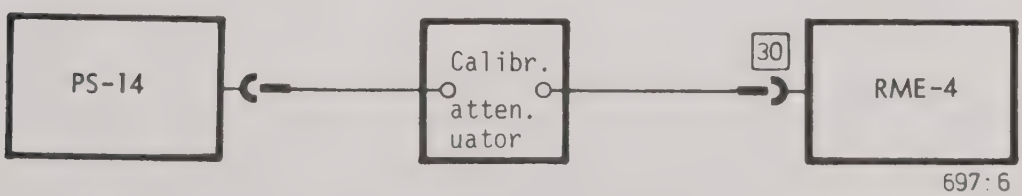


Fig. 9-14 Measuring set-up for Section 9.20.4.

Settings on the instruments:

PS-14: f = 100 kHz, level 0 dBm

RME-4: [29] (S 1601): BF level P_{BF}

[42] (S 3401): Middle setting, P_{BF}

- Plug card [697-CJ] onto adapter card [697-AT]. Connect digital voltmeter to Point M (+) and Point A (-) on the adapter card.
- Calibrate BF level meter
- Set calibrated attenuator to 50 dB attenuation and adjust output level (approximately 0 dBm) on the PS-14 so that the digital voltmeter indicates -1.000 V.
- Check all attenuators in accordance with the following table. Required voltage at Point M: -1.000 V $\pm$10 mV. If the tolerance range is exceeded, a correction can be made by changing the appropriate trimming resistors. Metal film resistors with TK 50 should be used for adjustment purposes.

Attenuation of the calibrated attenuator	Attenuator in the RF amplifier (32)	Corresponding trimming resistor
30 dB	20 dB	R 3222
40 dB	10 dB	R 3230
42 dB	8 dB	R 3249
44 dB	6 dB	R 3247
46 dB	4 dB	R 3245
48 dB	2 dB	R 3243
49 dB	1 dB	R 3213

9.20.5 ADJUSTMENT OF THE FREQUENCY RESPONSE

Measuring instruments required:

1 Milliwatt Power Meter with Test Probe 75 Ω	e.g. EPM-1 with TK-10	supplied by W&G
1 T-piece 75 Ω	e.g. BN 595/1	supplied by W&G
1 Level Generator	e.g. PS-14	supplied by W&G
1 Display Unit with Horizontal Amplifier SGH-22 Vertical Amplifier SGV-23	e.g. SG-2	supplied by W&G
1 calibrated attenuator	e.g. D 120	supplied by Siemens

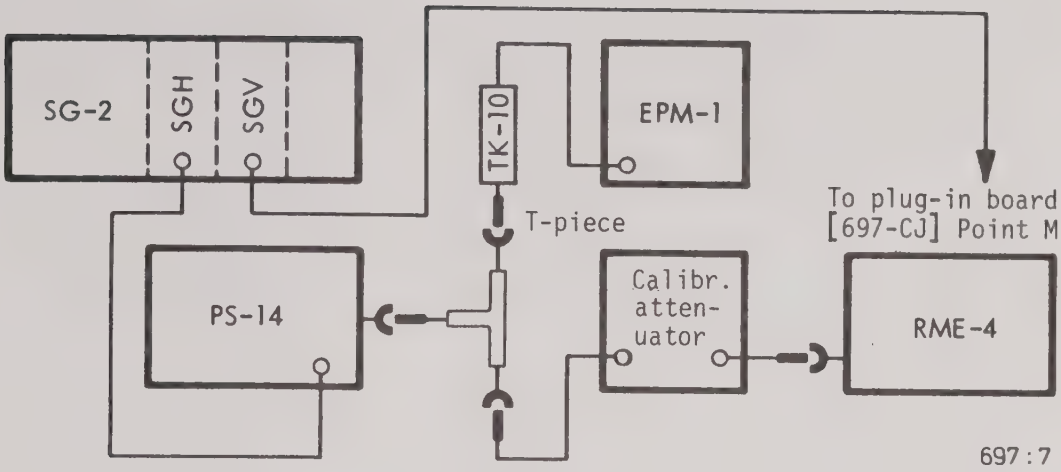


Figure 9-15 Measuring set-up for Section 9.20.5

Settings on the instruments:

EPM-1: Measuring range 0 dBm ±0.2 dB

PS-14: Level +6 dBm, sweep operation with f_{min} = 100 kHz and f_{max} = 14 MHz, sweep time 1 s.

SG-2: SGH-22 sensitivity 1 V/Div. Adjust position and expansion so that at f_{min} the beam deflects to the left-hand edge of the screen and, at f_{max}, to the right-hand edge. SGV-23 sensitivity 100 mV/Div. = 0.1 dB/Div.

RME-4: [29] (S 1601): BF level P_{BF}
[42] (S 3401): Middle setting, P_{BF}

- Set the sweep time on the PS-14 to "manual". Using the potentiometer, adjust the frequency "manually" from 0.1 to 14 MHz and read off the frequency response of the Generator on the EPM-1. The Generator frequency response thus obtained should be taken into account accordingly when adjusting the level meter. Reset sweep time to 1 s.

- Set calibrated attenuator to 40 dB attenuation (the 10 dB attenuator in the RF amplifier (32) comes into operation). Start sweep operation on the PS-14. Set frequency response in the range 1 to 5 MHz to minimum using C 3239 and set the frequency response in the range up to 14 MHz to minimum using L 3204. Requisite value in the range 0.1 to 14 MHz $\leqq$ 0.1 dB.

- Check and, if necessary, adjust the frequency response of the remaining attenuators in the RF amplifier (32) as shown in the following table and in the specified sequence.

Attenuation of the calibrated attenuator	Attenuator in the RF amplifier (32)	Corresponding trimmer capacitor
50 dB	-	C 3216
30 dB	20 dB	C 3210
42 dB	8 dB	C 3227
44 dB	6 dB	C 3225
46 dB	4 dB	C 3223

Required frequency response in the range 0.1 to 14 MHz $\leq$ 0.1 dB

10. DESCRIPTION OF THE FUNCTION

The appendix with the block circuit diagram and the individual circuit diagrams of the sub-assemblies is to be used as an aid for understanding the following sections.

In the detailed description of the sub-assemblies, the circled numbers in the section headings refer to the numbers of the circuit diagrams in the appendix.

10.1. Description of the Function by Means of the Block Circuit Diagram

10.1.1. IF Part

10.1.1.1. "Tracking" Mode of Operation

The IF input signal from socket [27] (Bu 1) reaches the input amplifier (7) over the calibration line. As a variable gain amplifier, this input amplifier (7) has the task of keeping the demodulator input level constant. A correction by more than 10 dB is possible.

From the input amplifier, the IF signal reaches mixer I, where it is converted with the carrier of the sequential oscillator (8) to 20 MHz. The 32 MHz low-pass filter (2) blocks the signal and carrier remainders.

The signal reaches mixer II (4) by way of the buffer amplifier, delay equalizer and attenuation equalizer. Mixer II (4) mixes the carrier signal (160 MHz) from component (12) with the 20 MHz IF to 140 MHz. The 152 MHz low-pass filter, which follows, is intended to attenuate the carrier remainder. The

140 MHz IF is supplied to the demodulator (27) via relay Rel 401, buffer amplifier (4) and relay Rel 402. The demodulated signal (test frequency) is distributed over the matching amplifier (5) to the following circuits:

- BB output socket [32] (Bu 501) with 50 mV/MHz
- To the BB part for measuring of distortion
- When operated with the speech equipment, the demodulated signal is supplied to socket [51] (Bu 1401) on the back panel of the instrument
- The test frequency is supplied to the deviation test rectifier (13) for measuring the deviation.

10.1.1.2. "Wideband" Mode of Operation

As already explained Section 10.1.1.1., the wideband IF signal reaches the input amplifier (7) .

In the case of an IF 140 $\pm$50 MHz, the signal at the output, regulated to constant level, is supplied to the demodulator (27) over the buffer amplifier (3) and the relay Rel 402. In the case of an IF of 70 $\pm$25 MHz, the signal from the output of the input amplifier (7) reaches a doubler (3) by way of a barrier amplifier (3) . The IF signal, doubled from 70 MHz to 140 MHz, reaches demodulator (27) via relay Rel 401, barrier amplifier and relay Rel 402.

With one exception (no evaluation in the BB part!), the distribution of the BB signal is the same as that described in Section 10.1.1.1.

10.1.1.3.Level Regulating Circuit

The level regulating circuit is intended to keep the demodulator input level constant. In order to keep the AM/PM conversion of the demodulator small, the regulating circuit must control the amplitude fluctuations of a component to be tested as a function of the sweep frequency.

The input level at socket W 11 is rectified in the modulator (27) and supplied to socket W 7 of the barrier amplifier (16). The control voltage at the output of the barrier amplifier (16) alters the amplification of the input amplifier (7) in such a manner that the input level of the demodulator remains constant.

10.1.1.4.Frequency Regulating Circuit

On changing the input frequency at socket [27] (Bu 1), the sequential oscillator (8) is so adjusted that there is a constant IF of 20 MHz at the output of mixer I (2).

The 20 MHz IF is supplied over the 32 MHz low-pass filter (2), the barrier amplifiers (2) and (9) over Bu/St 1106 to the 50:1 voltage divider in the auxiliary regulating circuit (11). It follows over St/Bu 1105 of the frequency/voltage converter in the main regulating circuit (10). At the output of the barrier amplifier (10), the regulating voltage, obtained in the frequency regulating circuit, controls the sequential oscillator (8). The sequential oscillator (8) oscillates at a frequency which is 20 MHz higher than the input signal.

From the output of the sequential oscillator, the carrier signal is supplied to the mixer I (2).

The 20 MHz IF must be regulated accurately to ±20kHz. This cannot be done only with the frequency/voltage converter in the main regulating circuit (10). The residual filing of the IF is corrected by the auxiliary regulating circuit (11). The 20 MHz IF at the output of the barrier amplifier (9) is divided by 100 (50:1 and 2:1) in the auxiliary regulating circuit (11), as is the 20 MHz crystal frequency of the crystal oscillator (25). The frequencies, divided into 200 kHz frequencies, are then compared digitally and the frequency difference is supplied to the frequency/voltage converter in the auxiliary regulating circuit (11). The regulating voltage of the frequency regulating circuit, so obtained, alters the reference for the regulating voltage of the frequency regulating circuit. The sequential oscillator (8) is readjusted until a difference is no longer supplied to the frequency/voltage converter in the auxiliary regulating circuit.

10.1.2. Absolute IF Level and Frequency Response Measurement

In wideband operation, the level at the input of the detector amplifier (7) is 10 dB greater than in tracking operation. In order to offer the same level to rectifier (7) in tracking and wideband operation, the amplification of the detector amplifier in the case of wideband operation is 10 dB lower than in the case of tracking operation. This is controlled by switch [36] (S 1401).

The rectified input signal is logarithmized in the indicator logarithmizer (13) and, in the case of the absolute level measurement, reaches switch X-Y (15) over push button [15] S 1503/I. The amplification of the indicator logarithmizer (13) can be adjusted with potentiometer [21] (P 1306) (CAL. P_1).

In the case of the measurement of the IF frequency response, the logarithmized signal is carried over push buttons [9] (S 2203) or [23] (S 2204) to the cross-fader (22).

A switching signal is carried into the indicator logarithmizer (13) in order to switch the bandwidth from 300 Hz to 6 kHz.

The LED indicator Gl 1303, Gl 1304 shows whether the DC voltage at the input of the logarithmizer lies outside the permissible range.

10.1.3. Deviation Measurement and Bessel Operation (Spectrum Analysis)

A BB voltage is available at the output of the demodulator. This is supplied over the matching amplifier (5) to the deviation measurement rectifier (13). It is possible to measure the r.m.s. in tracking as well as in wideband operation.

In the case of wideband operation with an IF of 70 MHz, the frequency deviation is also doubled by the frequency doubling in (3). This is compensated for by the division of the signal level with relay Rel 501.

The amplification for the test signal can be switched over in

the deviation measurement rectifier with push button [15] (S 1503/III) by so doing, deviation measurement ranges of 500 kHz and 2.5 MHz are obtained. The amplifier test voltage is rectified and subsequently reaches switch X-Y (15) over push button [15] (S 1503/1). The deviation indication can be calibrated with the help of the Bessel method and potentiometer [13] (P 1304).

In the case of the "Bessel" mode of measurement, the U_X generation (16) is switched with push button [15] (S 1503/11) to a frequency of 18 Hz. The reference of the main regulating circuit (10) is altered with the U_X voltage of component (16). The regulating voltage sweeps the sequential oscillator (8) with a deviation of about $\pm$0.6MHz. At the output of mixer I (2), the 20 MHz IF is also swept with $\pm$0.6 MHz. The swept 20 MHz IF arrives at mixer (9) over the 32 MHz low-pass filter (2), and the barrier amplifiers (2) and (9). The crystal oscillator (25) supplies the carrier signal of 20 MHz over St/Bu 1102 and St/Bu 1103. The output signal from mixer (9) is carried over the 20 kHz low-pass filter and push button [15] (S 1503/II) to switch X-Y (15).

The amplification of the output signal can be increased by a factor of 10 with push button [21] (S 901).

10.1.4. IF Return Loss Measurement

The output signal of the return loss measuring bridge comes to mixer III (17) from input [28] (Bu 1701). The carrier is fed into the mixer from the sequential oscillator (8). At the

output of the mixer (20 MHz), the signal is carried over the 20 MHz band-pass filter (17) into the logarithmizer (17). The logarithmized DC voltage at the output of the 20 MHz logarithmizer comes to the cross-fader (22) over switch [9] (S 2203) or [23] (S2204) and push button "ΔP_{II}".

10.1.5. BB Part

10.1.5.1. Evaluation of the Test Signal

The BB part of the RME-4, in which the evaluation of the distortion test results takes place, is synchronized automatically with the test signal, applied at the input [30] (Bu 1901) or coming from the output of the matching amplifier (5) with the test frequency f_M. After the 20 dB divider (19), the test signal is fed over St/Bu 1902 to the variable-gain amplifier in the frequency identification (23). The test frequency is identified and converted in the inter-wiring of the BB part (29) sub-assembly into a TTL signal. The control lines (TTL) for the 8 test frequencies affect the following self-assemblies:

- lamp control (14); indication of the respective test frequency with Gl 1411...Gl 1418; indication of the applicable transit time or phase test range with Gl 1501...Gl 1504
- preselection (19)
- selection (20)
- changeover of gain of the phase control circuit (24)
- crystal oscillator (25)

In addition, the test signal comes from St/Bu 1902 over two

consecutive selection circuits in the preselection (19) and selection (20) sub-assemblies to the rectifier (21) or the phase meter (24). The selection circuits are connected into the circuit according to the test frequency of the inter-wiring of the BB part (29) sub-assembly.

The amplitude fluctuation at the output of the rectifier are a measure of the slope distortions $\Delta U/U_o$ or of the differential amplitude caused by the component to be tested. The distortion test result reaches the cross-fader (22) over the test range switch [24] (S 2202), the $\Delta U/U_o$ amplifier (22) and push button [23] (S 2204/III).

The phase test result at the output of the phase meter (24) reaches the cross-fader over the test range switch [10] (S 2205), the $\Delta\varphi$ amplifier and push button [9] (S 2203/III). In the case of test frequencies <1 MHz, the phase test result is indicated as the group transit time $\Delta\tau$ in ns. Since the group transit time is however dependent on the test frequency, the gain in the $\Delta\varphi$ amplifier (22) is switched over depending on the test frequency. The gain applicable to the respective test frequency is signaled by the LED's Gl 1501... Gl 1503 at the front plate of the instrument. In the case of test frequencies >1 MHz, the test result is evaluated as the differential phase $\Delta\varphi$ in % rad, which is shown by the LED Gl 1504.

The cross-fader (22) enables two results to be represented simultaneously. One result of each of the push button rows [9] (S 2203) and [23] (S 2204) can be represented. At the same time, potentiometer [14] (P 2203) permits the brightness of the two test results shown to be adjusted in opposite directions. The results can be displaced in the Y direction with potentiometers [8] (P 2201) and [22] (P 2202). A calibration graticule can be superimposed with switch [2] (S 2201). The test results arrive in the reversing switch X-Y (15) over the array of pushbuttons [15] (S 1503/I and S 1503/II) and are supplied amplified to the display unit over Bu 104.

10.1.5.2. Amplitude Regulating Circuit

The amplitude regulating circuit regulates the voltage at the rectifier (21) to a constant value. On the one hand, it must be so slow that changes in test results with the deepest deflection frequency of 18 Hz are not leveled and, on the other, it must respond quickly when the test frequency is switched over.

In the preselection (19) sub-assembly, the test frequency is guided to a controlled amplifier. From there, it passes over a selective amplifier (selection (20)) and reaches the rectifier (21). Over an FET switch in (21), the control voltage of the amplitude regulating circuit adjusts the variable gain amplifier in such a manner that there is a constant level at the rectifier.

The FET switch in (21) is clocked with the deflection frequency.

The regulating circuit is closed about 50 µs in the center of image, that is, changes in the test results are related to the value in the center of the image.

10.1.5.3. Phase Regulating Circuit

The phase meter (24) compares the test frequency (from the selection (20)) with the reference frequency (crystal oscillator, sinusoidal/square-wave converter and divider (25)). The control voltage from the output of the phase meter is carried over a switchable amplifier in (24) to the crystal oscillator (25). The oscillator frequency is controlled to the same frequency and phase as the test frequency. At the same time, the regulating circuit is so sluggish, that the phase test results are not leveled out. The different slopes of the crystal oscillators are compensated for with the switchable amplifier in the phase regulating circuit (24).

10.1.5.4. Obtaining the U_x Signal and Further Response

The swept signal U_x for the display unit is obtained in a phase-regulated oscillator in the U_x producing sub-assembly (16). In the case of IF sweep measurements, the control voltage of the main regulating circuit (10), which is proportional to the sweep voltage, is used as reference. The control voltage is conducted over switch [29] (S 1601/I) into the position "IF" of the U_x generation (16).

In the case of BB sweep measurements, the swept voltage passes from socket [30] (Bu 1901) over the low-pass filter (19) and switch [34] (S1602) into the U_x generation (16). In the case

of the BB sweep measurements, the additional possibility exists of deriving the swept signal from an IF signal which is simultaneously conducted to the IF input [27] (Bu 1). At the same time, the control voltage from the main regulating circuit (10) is conducted over switch [34] (S 1602), the phase shifter (16) and switch [29] (S 1601/I) to the U_x generation (16).

The sinusoidal U_x signal at the output of the U_x generation is distributed to the following sub-assemblies:

- matching amplifier (5) ; the signal is required for the "retransmission of test results" mode of operation
- main regulating circuit (10) ; for the "Bessel" type of measurement
- rectifier (21) ; for the production of the control impulse
- recording assembly (26)
- to the display unit; over pushbutton [15] (S 1503/I) and the X-Y reversing switch (15)

For the $\Delta U/U_o$, $\Delta\varphi$ amplifier (22), the U_x generation (16) supplies a square-wave signal.

10.1.6. Marker Generation

10.1.6.1. Crystal Markers

The 20 MHz crystal frequency from the sub-assembly (25) is halved in the auxiliary regulating circuit (11) and subsequently conducted to the frequency marker sub-assembly (6). The frequency of 10 MHz is divided into 2 MHz or 5 MHz, depending on the position of the marker switch [11] (S 601).

A spectrum is obtained from this frequency and conducted to the following mixer. The carrier comes from the sequential oscillator (8). The beat markers are formed at the output of the mixer (6). These are concucted to the X-Y reversing switch (15) and superimposed to the Y signal. Switch [40] (S 1501) allow the choice of whether the markers shall be superimposed on the measured result or on the calibration line. Potentiometer [18] (P 1502) adjusts the markers height when the markers have been superimposed on the result.

10.1.6.2. Constant Markers

Two markers on the CRT screen of the visual unit can be displaced with potentiometer [25] (P 1610) and [26] (P 1611).

These square markers lead from the U_X generation (16) to the X-Y reversing switch (15). The marker heights can likewise be set with potentiometer [18] (P 1502) when the markers are superimposed on the result.

10.1.7. Recording Assembly (Accessory, Present Only if Requested)

All results, which can be represented on the CRT screen of the display unit with pushbuttons [9] (S 2203) and [23] (S 2204), can also be recorded with an X-Y recorder if the RME-4 is equipped with the recording assembly (26). The recorder can be started with pushbutton [19] (S 2602). The recording time can be varied between 2 s and 20 s with switch [12] (S 2602).

10.1.8 BF LEVEL METER (accessory, only supplied on request)

In operating mode P_{BF}, the BF level meter can be used to measure levels of -50 to -10 dBm in the frequency range 12 kHz to 14 MHz. In operating mode ΔP_{BF} it is possible to represent a level range of ± 1 dB on the display screen of the RME-4 for sine-shaped sweeping. The digital display then indicates the mean value of the swept BF level.

The input signal at socket [30] (socket 1901) passes through switches [29] (S 1601) and [42] (S 3401) to the input of the RF amplifier (32). When [42] (S 3401) is set to "Cal.", the 100 kHz calibration signal from the calibrated oscillator (34) is fed to the RF amplifier (32).

The input signal is amplified in the controllable RF amplifier so that the level at the output to the rectifier and discriminator (32) is almost constant. The dynamic range utilized at this point is still ±1 dB. The subsequent final amplifier feeds the rectifier with approximately 3 V_{pp}. The output voltage from the rectifier is routed through a 1-kHz low-pass filter and the DC voltage processing circuit to the logarithmizer (32). The logarithmized voltage is fed to the control circuit (33), the analog digital converter to the indication circuit (34) and to the Y-input for representation on the display screen during sweep operation.

The control circuit (33) controls the attenuators in the RF amplifier (32) in accordance with the input level. The attenuators are controlled so that the output voltage from the logarithmizer lies in the range 0...-2 V, provided that the input signal lies within the dynamic range of the level meter.

In the ΔP_{BF} operating mode for sweep operation, the control circuit (33) is blocked by switch [42] (S 3401). The attenuators information passes in parallel to the decoder (34) where it is recoded into level values and displayed after 7-segment decoding.

If the level range is exceeded or, alternatively, if it is not reached, the display circuit switches on LED Gl 3406 or Gl 3407, and simultaneously switches off the LCD display.

10.1.9 600 kHz LOW-PASS FILTER AND SATELLITE FILTER (accessories, only supplied upon request)

A 600 kHz low-pass filter (31) or a satellite filter (28) can be optionally incorporated in the connection between the output of the demodulator (27) and the input of the matching amplifier (5). The filters are inserted at plug-in connection St/Bu 502.

The 600 kHz low-pass filter (31) is necessary for measurements at 35 MHz IF in conjunction with the RMEU-4.

The satellite filter (28) is used for measurements in satellite systems. It contains a low-pass filter with approximately 600 kHz cut-off frequency as well as two band-pass filters for colour subcarrier frequencies of 3.58 MHz and 4.43 MHz.

Once inserted, the filter can be switched on or off using switch [38] (S 3101).

10.1.10 Display Unit ST-1 (See Separate Block Circuit Diagram in the Appendix)

10.1.10.1 External Supply Voltages

The display unit ST-1 is a panel-mounted instrument without its own power supply. The DC voltages for supplying the electronics (+5V, +12V, -12V) are delivered by the basic instrument RME-4. In addition, the display unit requires a DC voltage of +360 V for the sweep steps, as well as an AC voltage of 6.3 V for heating the picture tube. Since the heater coil is connected single-ended to -1.35 kV, the relevant winding of the mains transformer in the RME-4 as well as the wiring be isolated appropriately.

In addition, the supply voltage (about 4...5 V) for the graticule illumination is delivered by the basic instrument.

10.1.10.2. Internal Voltage Supply

In addition to the heater voltage, voltages of -1.25 kV (first accelerating voltage), +2.5 kV (second accelerating voltage) and -1.35 kV (for the brightness adjustment) are also required for the operation of the picture tube. The voltage of -1.25 kV is obtained from a voltage converter (consisting of a driving oscillator, an amplifier, a transformer and a half-wave rectifier). It is regulated since it has a great effect on the deflection factor of the picture tubes. An FET transistor, operated as a variable resistor, serves as a final control element.

The voltage of 2.5 kV is obtained by doubling the voltage from the AC voltage for -1.25 kV. Over a second secondary winding of the transformer and a halfwave rectifier, the voltage is changed from -1.25 kV to -1.35 kV.

The divider, with which the potential of the Wehnelt cylinder and therefore of the image brightness is determined, lies between -1.25 kV and -1.35 kV. If the electron beam is to be suppressed (for example, in the case of beam return), the Wehnelt cylinder is connected by the retrace blanking circuit to -1.35 kV and is then 100 V more negative than the cathode (-1.25 kV).

In order to supply the electronics of the retrace blanking circuit, a DC voltage of +7 V is produced from the heater voltage over a half-wave rectifier. For reasons of circuit engineering, the DC voltage of +7 V is converted to -1.35 kV.

10.1.10.3. Horizontal and Vertical Gain

The display unit does not have its own time base. The designs of the horizontal and vertical gain are largely identical. A limiting circuit protects the output stage in case the input signal is too large. By a two-step linearization circuit per image half, progressive as well as degressive imaging defects of the picture tubes can be offset. The output stage is designed as a bridge circuit. A constant current supply stabilizes the quiescent currents of the output stage transistors against fluctuations of the +360 V voltage and at the same time serves for supplying the divider for the astigmatism and geometry correction of the picture tubes.

The input signal for the warming-up protection circuit is taken at the output of the limiting circuit of the horizontal gain. Should the horizontal sweep signal be missing, this input signal connects the Wehnelt cylinder to -1.35 kV and so suppresses the electron beam.

The retrace-blanking signal for the beam return must be supplied by the basic instrument.

10.1.10.4. Picture Tube

The picture tube is an indirectly heated compact tube with a usable screen area of 80 mm X 100 mm. The sweep is electrostatic. A CRT screen with a very long afterglow duration (about 0.5 s until it declines to 10% of the initial brightness) also makes it possible for the sweep frequency to be low.

The overall acceleration voltage of 3.75 kV is composed of a first acceleration voltage of 1.25 kV (-1.25 kV cathode potential) and a post-acceleration voltage of +2.5 kV. By splitting the voltage into a negative and a positive voltage, it is achieved that the average potential of the deflecting plates (X and Y) is as low as possible (+14 V).

10.2. Detailed Description of the Sub-Assemblies

10.2.1. Power Supply (1)

The power supply consists of a standard power supply III, which is connected in series with an additional, altered standard power supply III. The power supply is mounted on the right

side wall of the instrument, the standard power supply being below and the altered standard power supply above.

The common mains input consists of a cold receptable, a line filter, a voltage selector, a mains on-off switch and a fuse. The AC voltages, transformed in the mains transformer to the individual secondary voltages, are rectified, filtered and conducted to the regulators (+5 V, ± 12 V, -14 V) or rectified and filtered (+360 V) or conducted as AC voltages to the mains output (4.2 V, 6.3 V). In the case of the 12 V and 24 V regulators, the auxiliary voltage for the controllers is tapped on the AC side of the supply voltage and conducted over its own rectifier and filter to the regulators.

The auxiliary voltage for the 5 V control is obtained from the regulated +12 V output voltage.

10.2.2. Mixer I, 32 MHz Low-Pass Filter, 20 MHz Amplifier, All-Pass Network (2)

10.2.2.1. Mixer I

At the signal input, the Mixer I receives either 70 ±25 MHz or 140 ±50 MHz. At the carrier input, there is a level of 500 mV, which is supplied by the sequential oscillator (8). The frequency of the carrier is approximately 20 MHz higher than that of the input signal. It is re-adjusted at the sequential oscillator (8), so that there is always a constant IF of 20 MHz at the output of the mixer.

In the amplification stage with T 202, R 210 is used for

adjusting the operating point and R 211 for offsetting the different attenuations of the two ring mixers IC 201 and IC 401.

The three stages T 201, T 202 and T 203 together have a gain of 10.8 dB, when R 211 = 309Ω. On request, the equipment can be supplied with R 240 and C 244 for increasing the frequency response.

10.2.2.2. 32 MHz Low-Pass Filter

The 32 MHz low-pass filter has the following non-pass attenuation:

from 60 to 300 MHz >60 dB and

from 100 to 200 MHz >80 dB

The transmission loss is <1 dB.

10.2.2.3. 20 MHz Amplifier

The 20 MHz amplifier consists of a two-stage amplifier with V = 8.1 dB for the decoupling and adjustment of the 32 MHz low-pass filter and the all-pass network, and a collector stage for coupling out the 20 MHz IF to the spectrum analysis (9).

10.2.2.4. All-Pass Network

The all-pass network sub-assembly may be divided into two parts:

- into the actual all-pass network, consisting of the two 33.8 MHz circuits L 208, C 237, C 239 and L 209, C 238 and the two 20.8 MHz circuits L 212, C 242 and L 213, C 243
- into the hole equalizer, consisting of the two 6 MHz circuits L 211, C 240 and L 210, C 241

The all-pass network and hole equalizer are used for correcting delay errors and frequency response errors in the IF path in the case of tracking operation.

10.2.3. Wideband Amplifier, Doubler (3)

The wideband amplifiers are used for the decoupling from the input amplifier. With an L signal at connection point 112, T 305 and therefore, over R 323, also T 304, are connected into the circuit. In wideband operation therefore, the negative operating voltage is switched on for T 301, T 302 and T 303.

The disconnection in tracking operation is necessary in order to achieve a high attenuation in the wideband path.

In wideband operation with an IF of 140 MHz, the input signal from connection point 114 arrives over T 301 at connection point 116 and plug ST 301.

In wideband operation at the IF of 70 MHz, the input signal from connection point 114 is conducted over the amplifier stages with T 302 and T 303 to connection point 115. It furthermore travels from connection point 109 over the frequency doubler IC 301 and over the amplifier stages with T 306 and T 307 to connection point 108 and plug ST 302.

In the frequency doubler, the input signal experiences a doubling of the frequency deviation but not of the sweep and test frequencies. In order to show the correct deviation, the output signal is halved in the matching amplifier (5).

10.2.4. Mixer II, 152 MHz Low-Pass Filter, 140 MHz Amplifier (4)

10.2.4.1. Mixer II

The mixer II receives a carrier frequency of 160 MHz from the fixed oscillator (12). A new IF of 140 MHz is formed with the 20 MHz IF at the signal input. The T 401 stage serves for decoupling and matching, while the T 402, T 403 stages amplify the mixer output signal by 7.4 dB.

10.2.4.2. 152 MHz Low-Pass Filter

The 152 MHz low-pass filter has a non-pass attenuation of 20 dB already at 160 MHz and, between 168 and 320 MHz, it is >30 dB.

The transmission loss is <2.5 dB.
All coils and a part of the capacitors are printed.

10.2.4.3. 140 MHz Amplifier

The 140 MHz amplifier is two-stage. Its amplification is 9 dB, when the output is under a load of 75Ω or of the demodulator (27).

The 140 MHz amplifier is in operation in the 70/140 MHz tracking and 70 MHz wideband modes. Switching over is accomplished with two HF relays.

The output voltage at connection point 68 is kept at a value of 265 $\pm$5 mV by level control in (16) and (17).

10.2.5. Matching Amplifier (5)

The matching amplifier brings the demodulator output signal of 44 mV/MHz to a level of 50 mV/MHz; this corresponds to an amplification of 1.11 dB. The amplified signal is available at the socket [32] (Bu 501) and is in addition conducted to the deviation measuring rectifier (13), the BB part (preselection (19)) and the speech equipment output [51] (Bu 1401).

The 15 MHz low-pass filter at the input is used for suppressing spurious lines and for improving the signal-to-noise ratio. The 6 dB divider which follows, when connected in the circuit over relay REL 501, cancels the deviation doubling in the case of "70 MHz wideband" mode.

The transistor T 503 forms the actual amplifier stage (current feedback). The operating point is set over a DC voltage negative feedback and kept constant. L 503 serve for correcting the frequency response.

In the "tracking" mode, a small deflecting voltage (residual deviation) is superimposed additively. In wideband operation, the residual deviation is switched off, that is, T 502 is blocked. The BB signal is conducted over the adjustable high-pass filter R 518, C 516, C 514 to the output stage T 504, T 506. In the case of a 50 Hz square-wave modulation, the tilt or sag can be corrected with the high-pass filter. The output stage is a degenerative amplifier with a 0 V DC output voltage. T 505 operates as a working voltage filter for the output stage. T 507 operates as power supply.

The output voltage of 0 V is achieved by the doubled transistor T 504. The voltage drop over R 518, R 519 and of the first base emitter diode is compensated by the second base emitter diode and R 525. For this purpose, equal emitter currents are necessary. They are set with potentiometer P 501. This adjustment is made possible by the fact that the emitter currents from T 504 are altered differently by the ring amplification R 521, R 528). The second transistor is bridged in AC fashion by C 518, R 526; as a consequence, $V \approx 1$ for the output stage.

Transistor T 508 serves for decoupling the BB part from the BB output [32] (Bu 501); at the same time, it operates as amplifier for the speech equipment.

P 502 allows the matching amplifier's white noise to be adjusted to a minimum value. After P 502 has been changed, the d.c. voltage at the BB output [32] should be again set to 0 V by P 501.

With C 529 any tilt in the $\Delta\varphi$ distortion can be corrected at 8.2 MHz.

10.2.6 Frequency Markers (6)

The frequency markers are derived from the carrier frequency for mixer I. This is higher than the input frequency by a constant frequency (20 MHz) and therefore is suitable for measuring the input frequency. For this purpose, the oscillator frequency is mixed with a spectrum of the appropriate marker frequency. Whenever the oscillator frequency exceeds a frequency line of the marker spectrum, a beat results at the mixer diode. This beat is amplified and formed into the frequency marker by the high and low-pass filters.

The crystal frequency of 10 MHz (connection point 37) is switched by a LOW signal at connection point 31 over IC 601/4.3 to a 5:1 divider and over IC 603/3.1 to T 601 or through a LOW signal at connection point 30 over IC 601/4.2 to a 2:1 divider and over IC 601/4.4 to T 601. A very rapid negative slope, with the marker frequency which has been set and which blocks Gl 601, stands at the collector of T 602. As a result of the stored charge of Gl 601, there is a short steep impulse with a uniform frequency spectrum at R 611. The oscillator frequency is supplied from connection point 38 over R 613 and C 608 and the marker spectrum is supplied over C 607 to the mixer

diode. The preconduction current for Gl 602 and therefore the amplitude of the beat can be adjusted with P 601. T 604 and T 608 operate as amplifier stages in grounded emitter circuit, T 607 as amplifier in grounded-base circuit and T 603 and T 609 as voltage followers.

When the 2 MHz frequency markers are switched in (LOW signal at point 31) resistors R 627 to R 628 are connected in parallel via IC 603/3.3 and T 605, and thereby the gain of T 608 is raised.

The external marker frequency is applied to point 33 and accordingly, through diode Gl 602, is mixed with the oscillator frequency.

10.2.7. Input Amplifier (7)

The input signal arrives at the common input (St/Bu 702) of the detector amplifier and of the input variable-gain amplifier by way of the IF input [27] (Bu 1) and the drum calibrating line EL 701. The calibrating line is built up from thin-layer attenuators and has a transmission loss of 0, 10 and 20 dB. R 726, L 702 and L 703 are used for matching to Z = 75 Ω, $r \leq 0.032$.

10.1.7.1 Detector Amplifier (Thin-film circuit DSS 703)

The detector amplifier is a degenerative wideband amplifier with a frequency range of 1.4 to 400 MHz (3 dB band width).

The amplification is switchable between V = 6 dB and 16 dB. The switching takes place in the degenerative feedback with a PIN diode current is adjusted with R 728 and P 707. The PIN diode is connected over T 706 of switch [36] (S 1401). In the "wideband" mode, a HIGH signal causes a small amplification because the input level is higher by 10 dB in the wideband operation.

The operating point of the second transistor is stabilized by a DC voltage degenerative feedback R 16, R 16 (DSS), R 734 and R 735.

The frequency response is corrected with C 9 (DDS), L 704 and C 726.

10.2.7.2 Detector Rectifier

The output signal of the detector amplifier (about 340 mV for full-scale deflection) is taken over R 743 and C 726 to the rectifier circuit.

The detector rectifier operates as a quasi r.m.s. value rectifier. The rectifier is constructed with a Schottky diode quartet.

The rectifier diodes are supplied over R 746 and P 704 with a preconduction current, so that small signals may also be processed.

In order to increase the accuracy (linearization), the DC voltage at T 708 is chopped and taken over the emitter sequence T 711, T 712 to an identically constructed rectifier. The output voltages of the test voltage rectifier Gl 703 and Gl 705 and of the second rectifier Gl 704 and Gl 706 are compared by the variable-gain amplifier IC 702, T 708.

The transistors T 709 and T 710 operate as choppers with a frequency of f = 200 kHz. The timing signal for T 709 comes over connection point 51 from the frequency divider in the auxiliary regulating circuit (11).

The chopped signal at the drain connection of T 710 is reformed by R 758, R 760, C 737 into an AC voltage, which has the same r.m.s. value as the corresponding sinusoidal voltage. The symmetrical construction of the rectifier provides good compensation of the temperature coefficients of the individual rectifiers.

The rectifier is balanced with P 703 (equalizing the different diode threshholds). Gl 707 and Gl 708 compensate the temperature coefficients of the bias (compensation of threshhold voltage changes of the two rectifiers Gl 703, Gl 705 and Gl 704, Gl 706 over the temperature).

C 735 short circuits residues of the chopper signal of T 710. C 734 and C 740 are used for stabilizing the regulating circuit. Their effect on the output voltage is compensated by C 749, C 750.

The output voltage is adjusted with P 706. The output voltage is conducted over connection point 45 to the display logarithmizer (13).

10.2.7.3. Variable-Gain Input Amplifier

The variable-gain input amplifier has a dynamics of about 14 dB (10 dB gradation of the calibrating line + 4 dB reserve). The input signal is conducted over the two amplifier stages T 705 and T 704 (emitter circuit with current feedback $V_{total} \approx 6$ dB) to the variable-gain amplifier T 703. The variable -gain amplifier is an emitter circuit with current feedback, which is supplied from a current supply T 702.

The PIN diode G1 701 operates as a positioning element in the degenerative feedback branch. The controlling voltage is produced in a wideband demodulator (27) and amplified on the U_x generation (16). The signal, regulated to a constant voltage, arrives over the buffer stage T 701 at the "mixer amplifier" thin-film circuit DSS 702. An oscillator circuit C 1, C 4 (DSS), L 706, L 707 with a resonance frequency of $\approx$210 MHz, which can be short circuited over the PIN diode

Gl 1 (DDS), is located in the emitter of the buffer stage. The oscillator circuit is used for suppressing a principle-induced interfering line in the "70 MHz" mode of operation. The PIN diode is switched over T 713 by switch [37] (S 1402). The output signal (120 mV) arrives over connection point 124 at mixer I (2).

10.2.8. Sequential Oscillator (8)

The sequential oscillator is a sweep oscillator, which produces the carrier frequency for mixer I in the sub-assembly (2) and for mixer III in the 20 MHz logarithmizer (17).

It is continuously tunable for the 70 MHz range of 65 to 115 MHz and for the 140 MHz range of 110 to 210 MHz, so that the IF of the RME-4 is always 20 MHz.

The oscillator with T 804 and T 808 is a unilateral, over C 808 and R 813 degenerative differential amplifier with series circuit L 801/L 803 and Gl 806 in the emitter circuit.

Range switching between 70 MHz and 140 MHz is accomplished with a TTL signal at connection point 58. LOW signal switches on T 803 and T 805 and blocks over Gl 803, T 807, T 806, Gl 804 and Gl 802. Accordingly, L 801 and L 803 are effective and oscillates in the 70 MHz range.

The HIGH signal blocks T 803 and T 805 and switches on T 807, T 806, Gl 804 and Gl 802. Gl 802 becomes very low-resistant and short circuits L 803; the oscillator oscillates in the 140 MHz range.

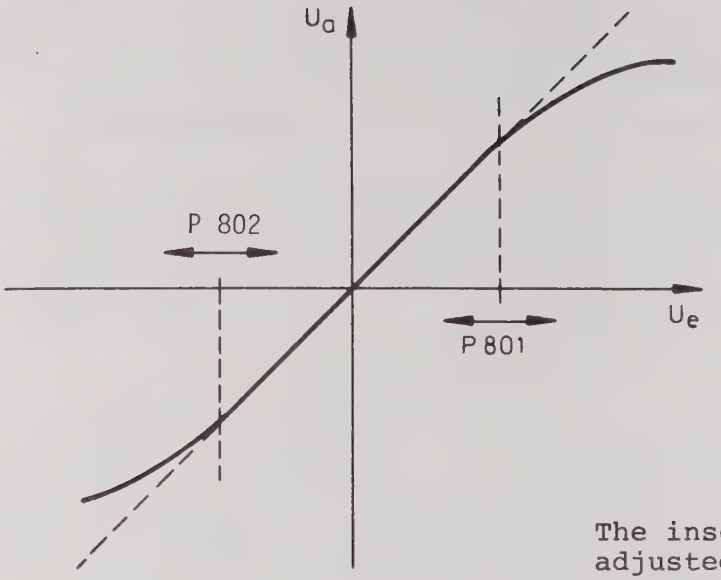
A HIGH signal at connection points 58 and 56 blocks all transistors from T 803 to T 807 and the oscillator is switched out of the circuit (wideband operation).

The continuous tuning takes place through Gl 806 over connection point 60. The divider from R 824, R 825, R 827 and C 814 makes it possible that the excitation at connection point 60 can take place approximately symmetrically about 0 V.

Because the modulation slope $\Delta f/\Delta U$ drops off inadmissably at the upper and lower ends of the band, the characteristic line must be linearized. This is accomplished by current impression: from T 809 for the lower end of the band and from T 810 for the upper end of the band.

The oscillator voltage is uncoupled over C 807 at the collector stages T 801 and T 802.

T 811, C 820, R 845, R 846 as well as T 812, C 821, R 847, R 848 form the operating voltage filters for low frequencies.



The inset points can be adjusted with P 801 and P 802.

Figure 10-1 Characteristic Line of the Oscillator

10.2.9. Spectrum Analysis (9)

10.2.9.1. 20 MHz Low-Pass Filter and Rectifier

The 20 MHz IF from component (2) arrives over T 903, the 20 MHz low-pass filter and the emitter follower T 907 at the rectifier Gl 903.

The differential amplifier T 909, T 910 is so adjusted with P 901 that, in the case of an IF of smaller 28 MHz, T 910 is turned on. This signal is supplied to the main regulating circuit (10) over R 942. In the case of an untrapped frequency and level regulating circuit, the input amplifier (7) regulates at full amplification. The level is limited with the diodes Gl 904 and Gl 905.

10.2.9.2. Bessel Function

The transistors IC 901/5.1 and IC 901/5.2, which are connected in the circuit as differential amplifiers, operate as mixers.

The signal (20 MHz IF) is supplied to the differential amplifier over the divider R 910, R 908. The carrier (20 MHz crystal frequency) is impressed over R 911 on the emitter current.

In addition to the crystal and the IF frequency, the product of emitter current through the transistor IC 901/5.2 and the differential voltage provides at collector IC 901/5.2 the difference frequency $U_o = \hat{U}_o \cdot \sin (\Omega - \omega) t$

$\Omega = 2 \pi \cdot f_{ZF}$; f_{ZF} = intermediate frequency

$\omega = 2 \pi \cdot f_Q$; f_Q = 20 MHz crystal frequency

C 912 attenuates the IF and the crystal frequency. In the case of the "Besseling" function, the IF is frequency modulated with 277 kHz (or 250 kHz), that is, there are sidelines at a distance of 277 kHz (or 250 kHz) about the IF. The IF is swept by about $\pm$ 0.6 MHz by the U_x generation (16). If the frequency is the same as the crystal frequency, a beat marker is formed (5 markers on the CRT screen).

Since the beats are formed at intervals of 277 kHz (or 250 kHz), it is necessary to make certain that the previous beat has decayed. This is accomplished with a 20 kHz low-pass filter of the third degree. The low-pass filter consists of the RC section R 916, C 912 and the active filter R 924, R 921, C 919, T 906, C 920. In the "Bessel" position of pushbutton [15] (S 1503/II)

the level of the beat marker is divided by about 10 over the divider R 932, R 933 and the transistor T 908, which is connected in the circuit. In the " X 10 " position of pushbutton [20] (S 901), T 908 is blocked.

From a certain level onwards, the beat markers are limited with the differential amplifier IC 901/5.3 and IC 901/5.4. This is necessary so as not to overdrive the display unit in the "X 10" position.

10.2.10. Main Regulating Circuit (10)

The task of the frequency regulating circuit is to control the sequential oscillator (f_o) in such a manner, that a constant intermediate frequency (f_{ZF}) of 20 MHz is maintained as the input frequency (f_E) changes. At the same time, the guide error should be as small as possible (only 0.5% $\hat{=}$ 46 dB in the case of the highest sweep frequency). At 100 Hz, the regulating circuit must have an amplification of more than 46 dB. Moreover, the test frequencies, lying on the input signal, must not be leveled out. That is, the regulating circuit must have a sufficient attenuation already at the lowest test frequency of 92.6 kHz (or 83.3 kHz). The second task is the recognition and trapping of the regulating circuit at each input frequency from 45 to 190 MHz. The IF of 20 MHz is divided in the auxiliary regulating circuit (11) into 400 kHz and supplied over connection point 78 to the discriminator in the main regulating circuit.

The operating voltage for the IC 1001 is adjusted to 5 V with P 1001. A deviation of the characteristic line of the

sequential oscillator (slope) can be offset with P 1002. The IF is adjusted to 20 MHz with P 1003.

After the frequency/voltage conversion in the discriminator, the voltage is supplied over IC 1005, IC 1007, IC 1008 and connection point 74 to the sequential oscillator (8).

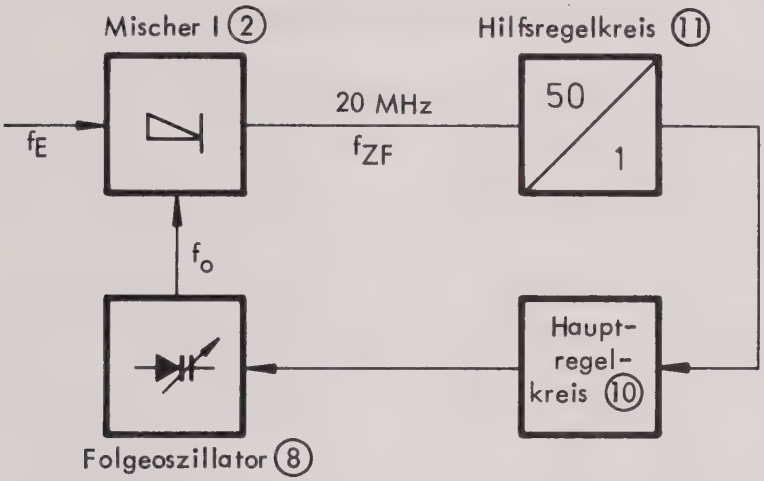


Figure 10-2 Simplified Block Circuit Diagram of the Frequency Regulating Circuit

Key for Figure 10-2:

Mischer	=	Mixer
Hilfsregelkreis	=	Auxiliary regulating circuit
Folgeoszillator	=	Sequential oscillator
Hauptregelkreis	=	Main regulating circuit

10.2.10.1.Discriminator

The discriminator (in the case of 400 kHz) consists of the monoflop IC 1001, the current supply IC 1002, T 1002 and the charging capacitor C 1006.

During the down-time T_p of the monoflop IC 1001, the diode G1 1001 blocks and the current I_o flows through R 1015 and provides a voltage U_a. In the rest time, I_o flows in the monoflop.

$$U_a = I_o \cdot R\ 1015 \cdot T_p \cdot f \longrightarrow U_a = k \cdot f$$

A frequency/voltage conversion is achieved with the discriminator.

10.2.10.2. Time Constants of the Regulating Circuit

The behavior of the regulating circuit is shaped by the following time elements:

- double integrater R 1051, R 1056, C 1012 and C 1014
- staircase element R 1036, R 1038 and C 1011
- element of the second order R 1062, C 1017, C 1018 and L 1001

The sequential oscillator (8) operates in the 70 and 140 MHz ranges.

Because the slopes are different, they are adjusted in the regulating circuit by the change-over switch of the amplification (IC 1007 and T 1009).

140 MHz $\hat{=}$ HIGH at connection point 77

70 MHz $\hat{=}$ LOW at connection point 77

Oscillating circuit L 1002, C 1025 attenuates the regulating circuit at the lowest test frequencies of 83.3 kHz or 92.6 kHz.

10.2.10.3. Trapping Circuit

In the "trapping" mode of operation, the receiver automatically

rests with the help of a trapping circuit at the applied IF input signal f_E when the instrument is switched into the circuit. in the not-rested state, the intermediate frequencies

$f_{ZF1} = f_o - f_E$ when $f_o > f_E$

and

$f_{ZF2} = f_E - f_o$ when $f_o < f_E$

are possible when mixing the input frequency f_E with the frequency f_o of the sequential oscillator (8).

In order to prevent the frequency regulating circuit receiving a wrong control direction, the second case must be excluded. For this reason, the sequential oscillator (8) is drawn to its highest frequency at the start of the frequency search run, as a result of which the IF of the output of mixer I (2) becomes greater than 20 MHz.

The trapping circuit is connected with the FET switch T 1007 over T 1008 and T 1010 parallel to the main regulating circuit. The regulating circuit closes over IC 1006, T 1007, IC 1004, IC 1005, IC 1007 and IC 1008.

The output voltage of IC 1008 follows the charging voltage at C 1013. The time constant is selected so that, on reaching the 20 MHz IF, all capacitors in the main regulating circuit are charged. Accordingly, the trapping circuit is built up correctly when the trapping circuit is separated.

The search run is explained by Figures 10-3 and 10-4. At the start of the search run, the IF at the output of mixer I (2) is

greater than 32 MHz (in Figure 10-4: Section A to B). However, because of the 32 MHz low-pass filter (2), the IF is blocked. The frequency comparator in the auxiliary regulating circuit (11) therefore supplies the information "IF too low". Since this is a wrong information, the calling key flip-flop IC 1010/3.1 and 3.2 is released only when the IF has reached approximately 28 MHz (Figure 10-4: Section B to C).

The IF is conducted over a low-pass filter (≈28 MHz) in the spectrum analysis sub-assembly (9) and subsequently rectified. When the IF has fallen below 28 MHz, the calling key flip-flop IC 1010/3.1 and 3.2 is released with a TTL signal from the spectrum analysis (9) over the inverter IC 1009/4.4 (Figure 10-4: Connection Point C). Furthermore, gate IC 1010/3.3 is released.

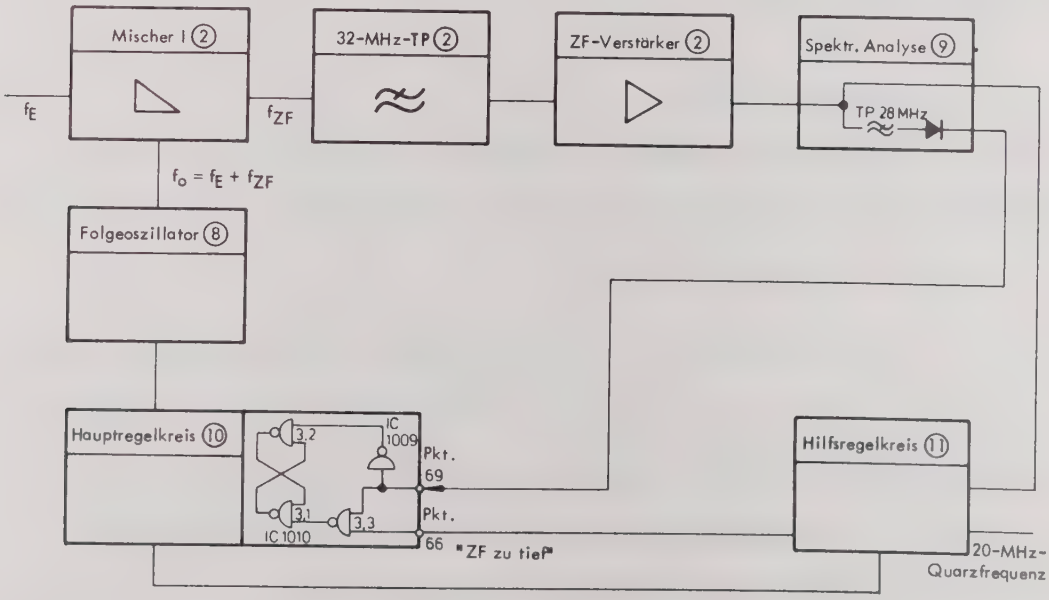


Figure 10-3: Simplified Blocked Circuit Diagram of the Frequency Regulating Circuit During the Search Run

Key for Figure 10-3:

Mischer	=	Mixer
ZF Verstarker	=	IF amplifier
Spekt. Analyse	=	Spectrum analysis
Folgeoszillator	=	Sequential oscillator
Hauptregelkreis	=	Main regulating circuit
ZF zu tief	=	IF too low
Hilfsregelkreis	=	Auxiliary regulating circuit
Quarzfrequenz	=	Crystal frequency

If the IF falls below 20 MHz (Figure 10-4: Connection Point D) the auxiliary regulating circuit (11) supplies impulses over connection point 66, which set the calling key flip-flop IC 1010/ 3.1 and 3.2. At low-pass filter 1009, there is 0 V $\hat{=}$ search run ended. The transistor T 1007 is blocked and the main regulating circuit has caught.

The search process is repeated with 3 to 9 Hz. At the same time, C 1013 is discharged over T 1012, T 1017 by the unstable monoflop T1018, T 1019.

The search process over T 1012, T 1013 and IC 1009/4.2 is not initiated in the case of wideband operation (HIGH at connection point 68) or in the case of a wrong input level of the RME-4 (HIGH at connection point 67).

The regulating circuit is prevented from locking itself by the differential amplifier. T 1016 blocks if the output voltage at

IC 1008 becomes more positive than + 7 V. At IC 1010/3.2, connection point 13, there are 0 V and at IC 1010/3.2, connection point 12, there is a HIGH signal. The search process is initiated. Moreover, the search process is initiated when the output voltage at IC 1008 becomes more negative than - 7 V.

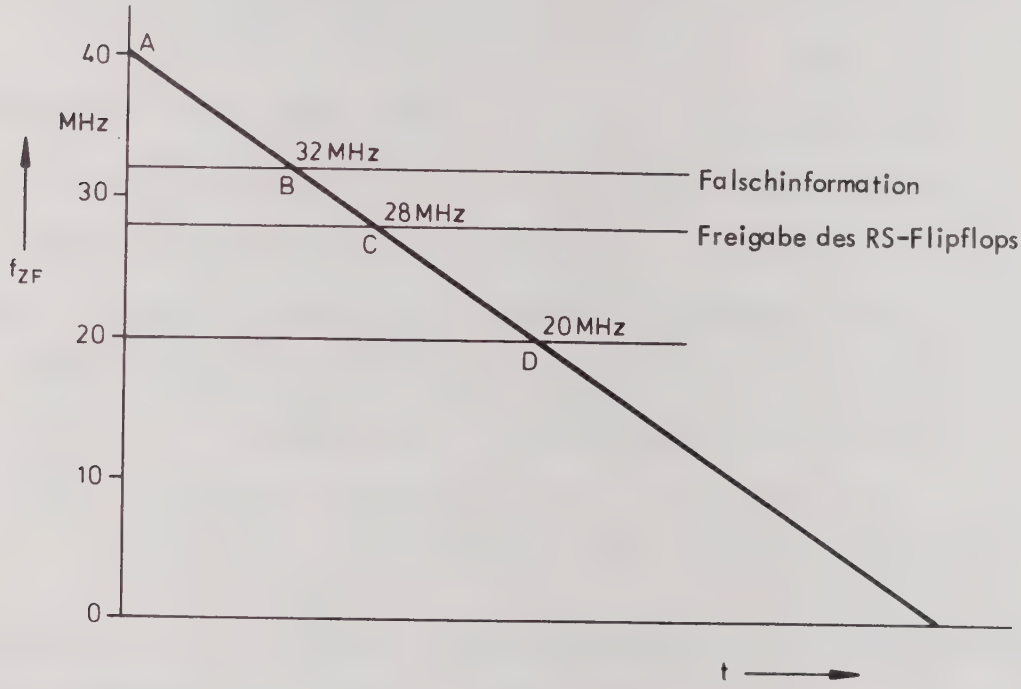


Figure 10-4 Behavior of the IF During the Search Process

Key for Figure 10-4:

Falschinformation	=	Wrong information
Freigabe des RS-Flipflops	=	Release of the calling key flip-flop
f_{ZF}	=	f_{IF}

10.2.10.4. Supplying the Auxiliary Regulating Circuit

In the auxiliary regulating circuit (11), the IF of about 20 MHz is compared with a crystal frequency of 20 MHz. The residual frequency deviation is removed from the auxiliary circuit by changing the reference at IC 1005 with a control voltage at connection point 71.

10.2.10.5. Supplying the Spectrum Analysis

In the "Bessel" mode of operation, the IF is altered by about ± 0.6 MHz with 18 Hz sine. This is accomplished by changing the reference at IC 1005 with a voltage at connection point 75. At the same time, T 1004 is connected in the circuit when there is a HIGH signal at connection point 80.

10.1.10.6. Speech Operation

Speech communication can be entered into over a distance with the speech equipment of the RM-4. The frequency control circuit of the receiver partially levels the speech frequencies from 1 to 5 kHz and therefore is not suitable for speech transmission. The regulating circuit is therefore switched over during speech operation.

C 1022 is connected parallel to the double integrator by means of the FET switch T 1020. The double integrator becomes an integrator with a zero passage of the regulating circuit at 70 Hz.

The FET switch is turned on by the speech equipment by pressing the speech pushbutton (Bu 1401/3 over T 1022).

10.2.11 Auxiliary Regulating Circuit (11)

The RME-4 recognizes the frequency at the input socket. The main regulating circuit (10) controls the sequential oscillator (8) so that, as there is a change in the input frequency, a constant intermediate frequency of about 20 MHz is maintained. The accuracy of this IF is determined by the discriminator of the main regulating circuit.

The remaining deviation is controlled by the auxiliary regulating circuit (11). In so doing, the IF is compared with a 20 MHz crystal frequency and the output voltage of the integrator IC 1113 is supplied over connection point 36 to the main regulating circuit for the purpose of further adjustment.

The IF is taken over connection point 42 to the comparator IC 1114. The subsequent 10:1 dividers IC 1102 and IC 1111 divide the IF into 200 kHz.

The crystal frequency of 20 MHz from connection point 40 is divided into 200 kHz by the 10:1 dividers IC 1102 and IC 1104. The crystal frequency, which has been divided 2:1, is taken at connection point 38 to the marker generation.

When the IF is lower than the crystal frequency, impulses are supplied to the main regulating circuit over connection point 33 (recognition as the main regulating circuit catches).

The discriminator of the main regulating circuit operates at

400 kHz. The 20 MHz IF is divided with the 10:1 divider IC 1112 and the 5:1 divider IC 1111 to 400 kHz and taken over connection point 41 to the main regulating circuit (10).

10.2.11.1. Shadow Region Production

In order to assure a reliable operation of the frequency comparator, the impulse arrangement of the two frequencies must be guaranteed.

The shadow region prevents impulses reaching the frequency comparator simultaneously, and so prevents the latter from giving a false signal.

The above is explained by means of Figures 10-5, 10-6a and 10-6b. When the points (B) and (D) carry a HIGH signal, the flip-flop IC 1107/2.1 is set to zero over the gate IC 1106/4.2. The gates IC 1108/2.2 and IC 1108/2.1 both become blocked. Neither impulse is evaluated.

It can be seen from the impulse plans in Figures 10-6a and 10-6b that:

- there is no overlapping of impulses at (B) and (D). The impulse at (H) is transferred to output (L)
- in the case of an overlap of impulses at (B) and (D) (shadow region), no impulse reaches the outputs (L) or (J)

The residence time of the monoflop IC 1103/2.1 must be greater than that of the monoflop IC 1105/2.2 and the residence time of the monoflop IC 1105/2.1 must be greater than that of the

monoflop IC 1103/2.2. (the residence times of the monoflops IC 1103/2.1 and IC 1105/2.1 are about 650 ns).

If this is not the case, the frequency comparator is driven with a faulty impulse. This case occurs when impulses follow one another in close succession from f_1 and f_2.

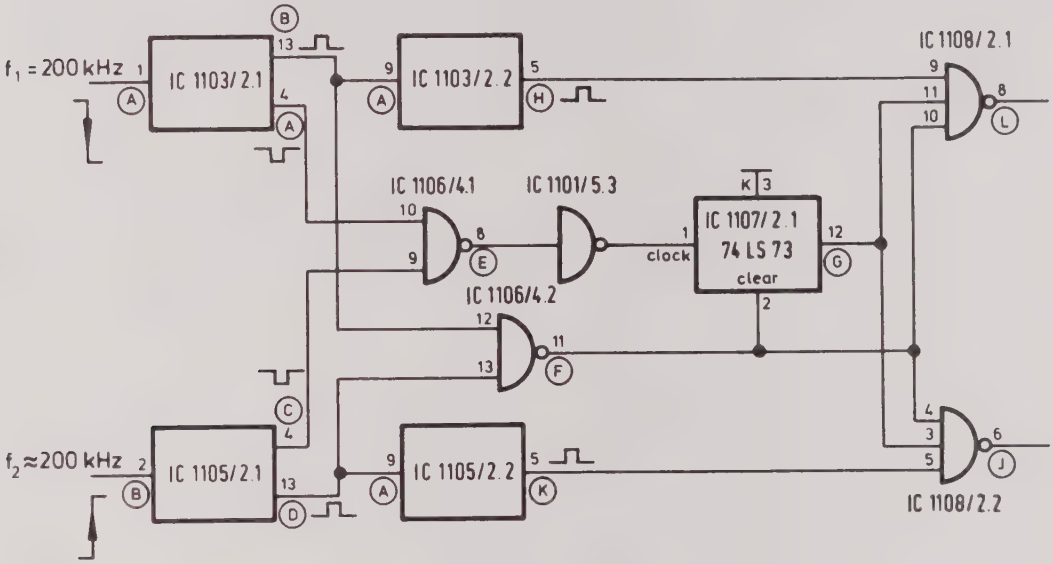


Figure 10-5: Shadow Region Generation in the Auxiliary Regulating Circuit

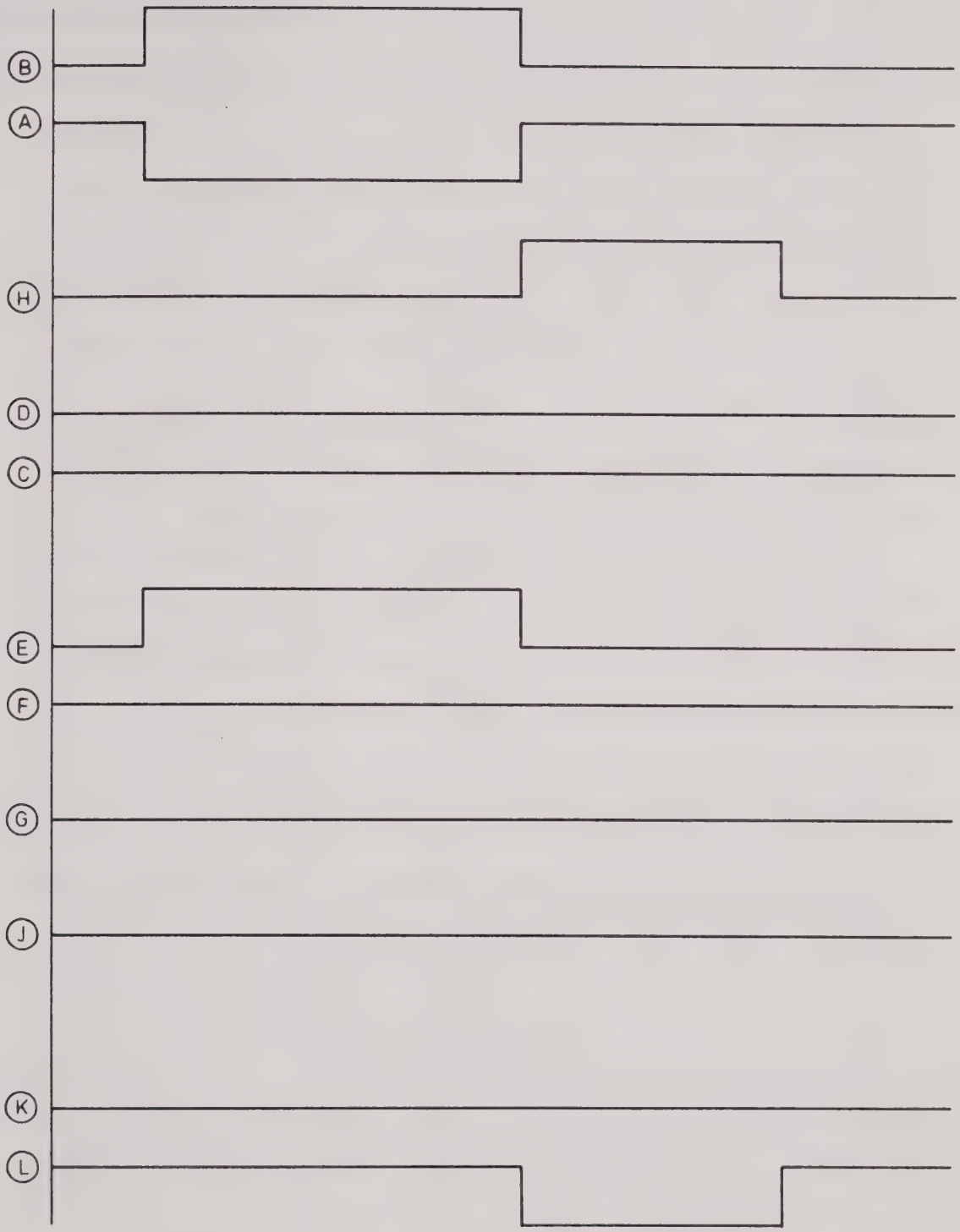


Figure 10-6a: Impulse Plan Shadow Region Generation: No Overlapping of the Driving Impulses (B) and (D).

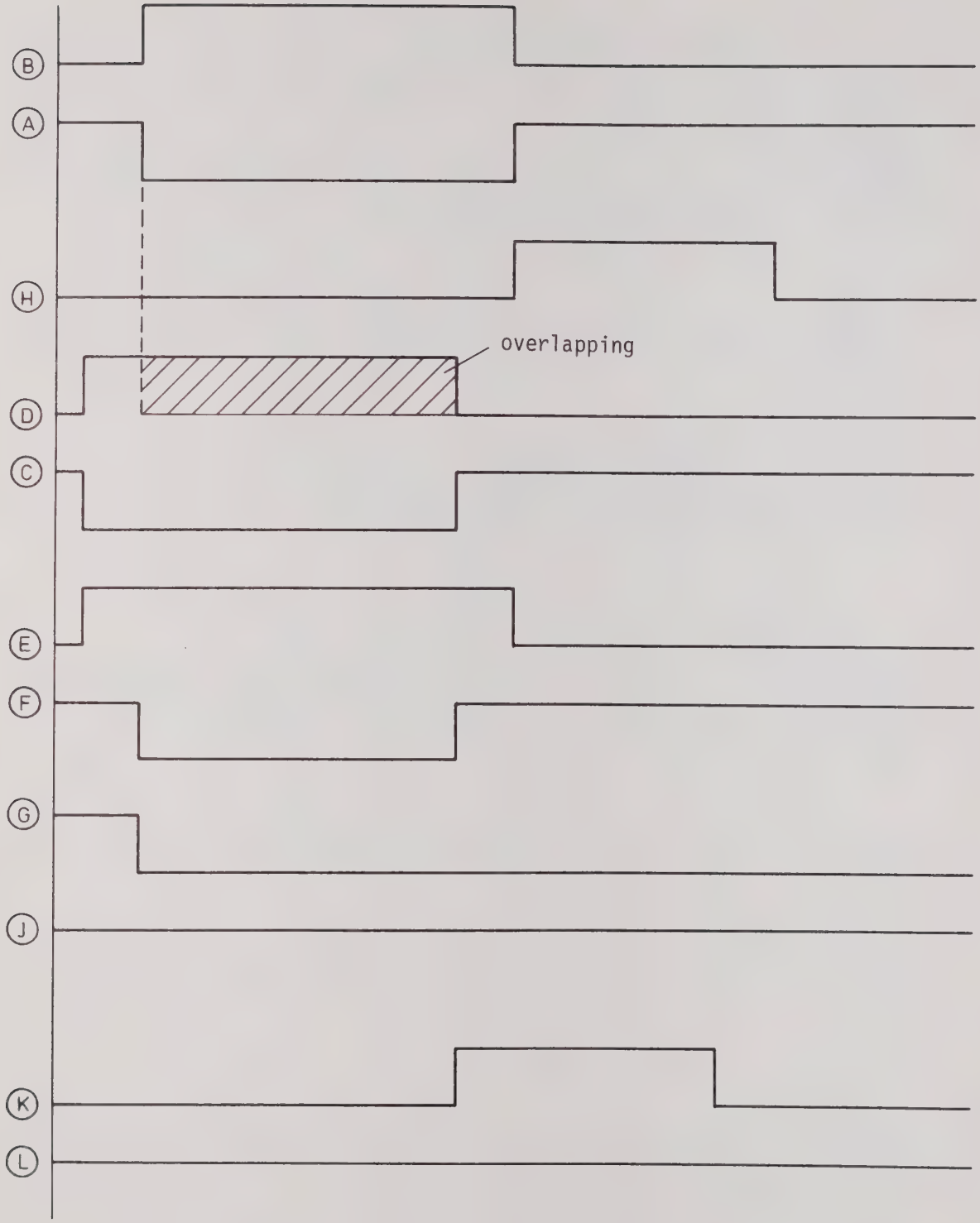


Figure 10-6b: Impulse Plan for Shadow Region Generation:
Overlapping of the Driving Impulses (B) and (D)

10.2.11.2. Frequency Comparator

The function of the circuit can be recognized from the excerpt of the circuit in Figure 10-7 and from the impulse plans in Figures 10-8a and 10-8b. In Figure 10-8a, the frequency $f_2 > f_1$ and in Figure 10-8b, $f_2 \approx f_1$. Both impulse plans are excerpts from an impulse process. The phase displacement appears to be constant only in this small section.

$f_2 > f_1$: The flip-flop IC 1107/2.2 is set with the impulse at (A) (output (D) on HIGH). This is followed by an impulse at (B), which resets the flip-flop into its original state. With a third impulse, it is again the turn of (B). This cannot set the flip-flop because the gate IC 1106/4.4 is blocked. The gate IC 1109/4.3 is however set free for the impulse at (B). At (J) there is an impulse. Each second impulse at (B) can pass the gate 1109/4.3, that is, $f_2 = 2 \cdot f_1$.

$f_2 = f_1$: It can be seen from the impulse plan in Figure 10-8 that, in the case of frequency equivalence, the flip-flop IC 1107/2.2 is set and reset on each occasion. There is no impulse at the outputs (H) and (J).

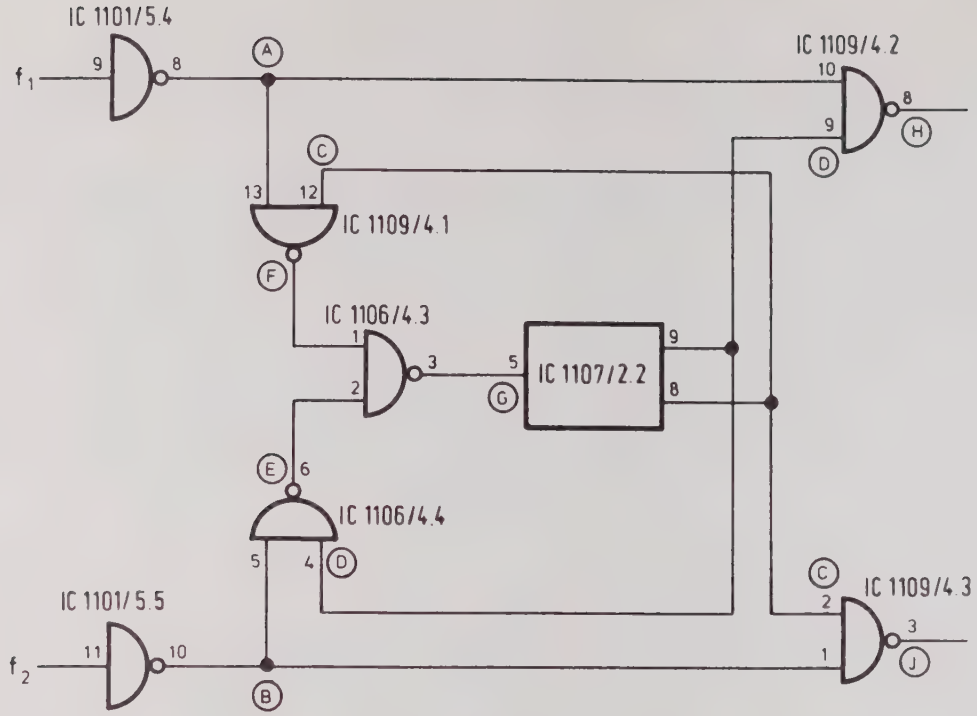


Figure 10-7: Frequency Comparator in the Auxiliary Regulating Circuit

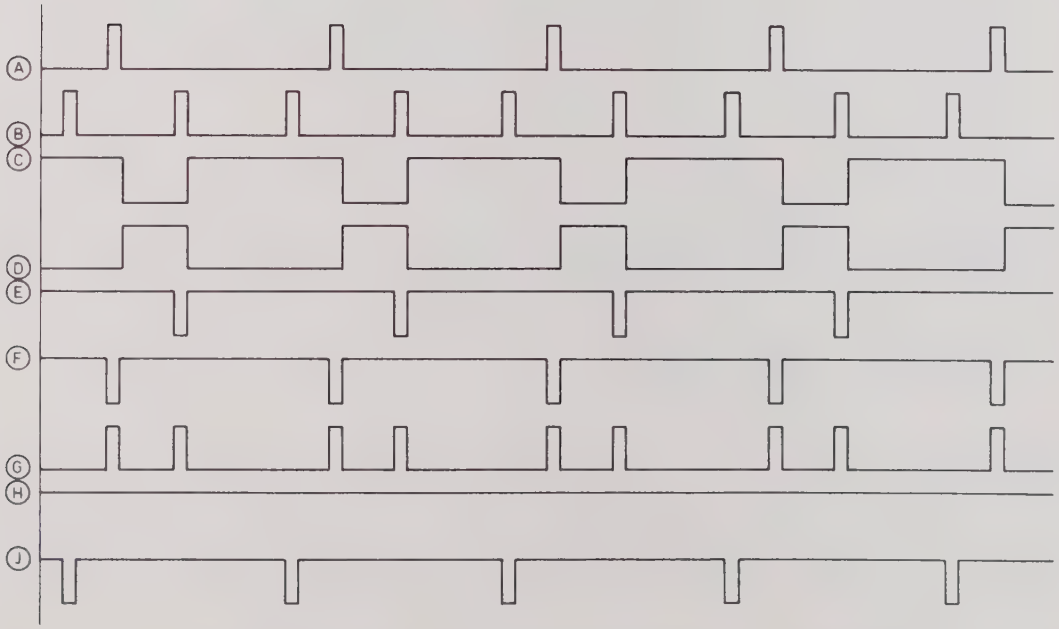


Figure 10-8a: Impulse Plan for Frequency Comparison: $f_2 > f_1$

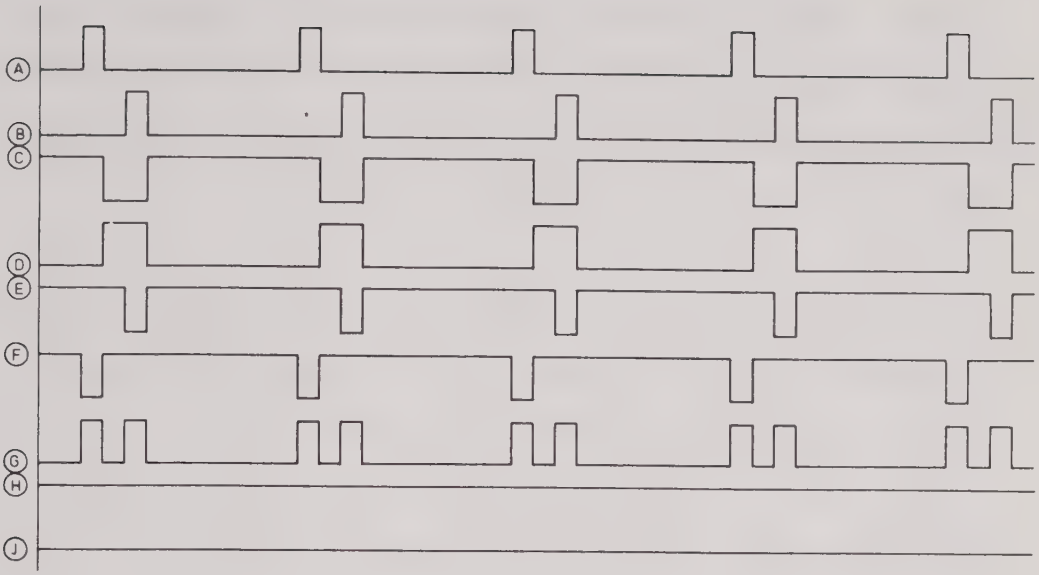


Figure 10-8b: Impulse Plan for Frequency Comparison: $f_2 \approx f_1$

10.2.11.3. Integrator

In the case of frequency indication, the monoflops IC 1110/2.1 and 2.2 on each occasion supply 5 µs impulses at the outputs, and moreover with a positive polarity at output 5 and a negative polarity at output 4.

There are impulses over R 1130 and R 1131 as shown in Figure 10-9.

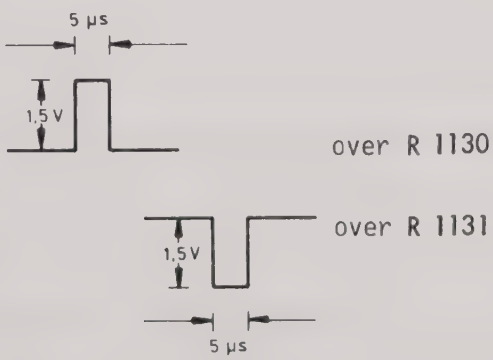


Figure 10-9: Impulse at the input of IC 1113.

These impulses recharge the integrator IC 1113, C 1116. The resulting output voltage at connection point 36 is supplied to the main regulating circuit (10).

10.2.12. Fixed Oscillator of 160 MHz (12)

The carrier frequency of 160 MHz for the mixer II (4), for bringing the IF of 20 MHz to the demodulator frequency of 140 MHz is produced in the fixed oscillator.

The oscillator with T 1201 and T 1203 is a push-pull oscillator with an oscillating circuit in the collector circuit. The ferrite beads L 1201, L 1202, L 1205, L 1206 are used for decoupling and prevent high-frequency oscillations.

The coupling out is high-resistant and takes place at a tap of the inductance over T 1202 at connection point 81.

10.2.13. Deviation Measuring Rectifier (13)

10.2.13.1. Deviation Measuring Rectifier

The deviation measuring rectifier operates as an r.m.s. value rectifier. The input signal is amplified by T 1301 and taken over T 1302 to the rectifier. The diodes of the rectifier are supplied with a preconduction current so that smaller signals may also be processed.

In order to increase the accuracy (linearization) the DC voltage at the collector of T 1303, which is proportional to the test voltage, is chopped and supplied over T 1306 and T 1307 to a rectifier designed like that for the test voltage. The non-inverting input of th

operational amplifier is positioned at the second rectifier. A very good temperature behavior is achieved through the symmetrically constructed rectifiers, because the diode voltages of the diodes Gl 1302/6.1 and Gl 1302/6.4 are compensated by the diodes Gl 1302/6.2 and Gl 1302/6.3.

T 1304 and T 1305 operate as choppers at f =200 kHz. The square-wave signal at the drain connection of T 1304 is transformed by R 1331, R 1332, C 1310 and C 1321 into a sinusoidal signal.

The preconduction current is set with P 1302 and the symmetry (diode threshhold adjustment) of the two rectifiers with P 1301. The output voltage is adjusted with P 1305.

For the deviation measuring ranges of 500 kHz and 2.5 MHz, the amplification of the emitter stage T 1301 is changed over by a factor of 5 with relay Rel 1301.

0.2.13.2. Display Logarithmizer

The display logarithmizer logarithmizes the output voltage of the display rectifier (7) and has a dynamic of 10 dB.

The current through R 1337 is logarithmized by T 1308. Accordingly, the voltage at IC 1303, Pin 6 is $U_D = U_T \cdot \ln(I_D/I_o)$.

T 1308 provides for a DC voltage offset, which is determined by R 1347. The logarithmized voltage is amplified by IC 1307 and IC 1308. The amplification is set with potentiometer [21] (P 1306) and the zero point with P 1307.

For the sweep measurement ΔP_I, IC 1309 amplifies the logarithmized voltage by a factor of 19 for the test ranges of 0.2 dB/division and 0.5 dB/division. The band width here is 300 Hz or

6 kHz, when T 1309 is conducting or blocked.

When the input level falls below or exceeds the dynamic range of the logarithmizer by 2 dB, the comparator IC 1304 or IC 1305 becomes active and switches on the light-emitting diode Gl 1303 (too low) or Gl 1304 (too high).

10.2.14. Lamp Control (14)

The RME-4 automatically detects the test frequency. The corresponding component is the frequency detector (23). The test frequency detected connects the associated LED indicator into the circuit of the lamp control with a TTL signal: Test frequency on $\hat{=}$ 0 V (connection points 12, 14 ... 18, 20 and 21).

The X-Y recorder is controlled in the X direction with the respective test frequency. The voltages of 0 V; 1.2 V; 2.4 V;...; 8.4 V are available at connection point 19 for recording with 8 test frequencies and recorder sensitivity of 0.4 V/cm.

Through the divider R 1424, R 1426, there is +1 V at IC 1403 Pin 3. Such an arrangement assures that the diodes Gl 1405 to Gl 1410 and Gl 1419 are securelyblocked at the lowest test frequency. Provisions are made with R 1421 that there is 0 V at connection point 19 for this frequency. At the next test frequency (277 kHz or 250 kHz) gate IC 1404/6.1 blocks (open collector), and a current, which provides a voltage of +1.2 V at connection point 19, flows over R 1436, Gl 1405 and through R 1419. The process is similar at other test frequencies.

Relays in the 140 MHz amplifier (4) are controlled with transistors T 1402 and T 1403. Transistor T 1402 is connected in the circuit in the "70 MHz wideband" mode of operation and transistor 1403 in the "140 MHz" mode of operation.

10.2.15. Reversing Switch X-Y (15)

The reversing switch X-Y is used for indicating simultaneously the test deviation Δf on the X axis and the level P_I on the Y axis of the display unit.

The process is as follows:

Process Phase 1: Deviation display Δf (see Figure 10-10).

The reversing switch X-Y is in the X position.

Then

- there is switching over between the reference line and the test result on the X axis and
- traces are written on the Y axis with a delta voltage.

Process Phase 2: Level Indicator P_I (see Figure 10-10)

The reversing switch X-Y is in the Y position.

Then

- there is switching over between the reference line and the level result on the Y axis and
- traces are written on the X axis with a delta voltage.

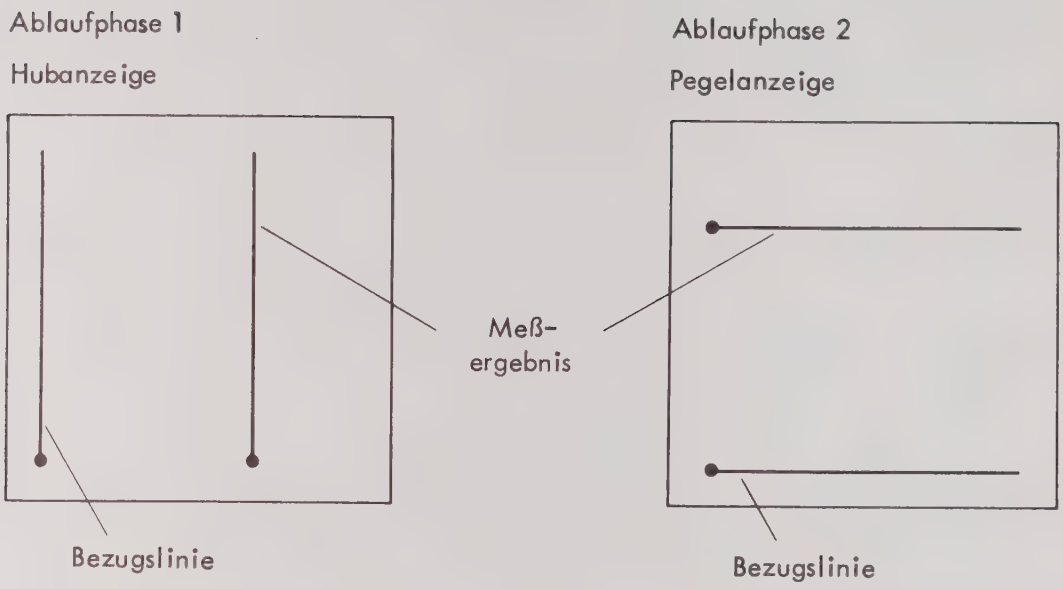


Fig. 10-10: Representation of the IF r.m.s. deviation and level on the display unit

Key for Figure 10-10:

Ablaufphase	=	Process phase
Hubanzeige	=	Deviation indication
Pegelanzeige	=	Level indication
Messergebnis	=	Test result
Bezugslinie	=	Reference line

During the switching over between process phases 1 and 2 as well as between the reference line and the test result, the beam is scanned dark.

The method of functioning is shown in the following block circuit

diagram. The inpulse plans in Figures 10-12a and 10-12b also help to explain the method of functioning.

The unstable multivibrator consists of the transistors T 1503, T 1504. It supplies the signal over the switching stage T 1502 and the divider IC 1503 to the divider IC 1504. The divider is switched off except for deviation (Δf) and level (P_I) measurements.

The delta former is composed of the integrating element R 1515, P 1501, C 1507, C 1508 and the voltage follower IC 1505. The amplitude of the delta can be adjusted with P 1501.

The reference line/test result reversing switch and the X-Y reversing switch are realized with FET switches in conjunction with transistors. In design, they are all the same; a transistor, whose emitter is positioned at a stable voltage of 6.1 V, is controlled by a TTL signal, so that it switchs through the FET switch. The stable voltage supplies T 1505, which is connected in the circuit as a voltage source.

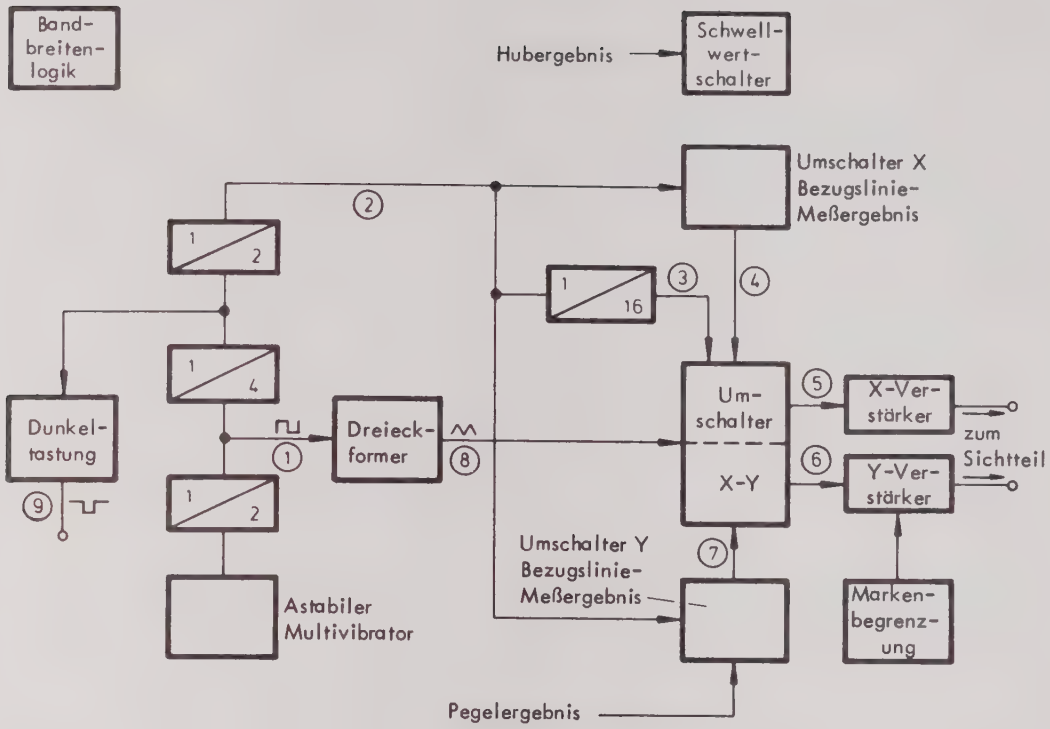


Fig. 10-11: Block circuit diagram of the X-Y reversing switch

Key for Figure 10-11:

Bankdbreitenlogik	=	Bandwidth logic
Hubergebnis	=	Deviation result
Schwellwertschalter	=	Threshhold value switch
Umschalter X	=	X reversing switch
Bezugslinie-Messergebnis	=	Reference line/test result
Dunkeltastung	=	Blanking
Dreieckformer	=	Delta former
Umschalter X-Y	=	X-Y reversing switch
X-Verstärker	=	X amplifier
Y-Verstärker	=	Y amplifier

Key for Figure 10-11 Cont.:

zum Sichtteil	=	To the display unit
Astabiler Multivibrator	=	Unstable multivibrator
Umschalter Y	=	Y reversing switch
Markenbegrenzung	=	Marker limitation
Pegelergebnis	=	Level result

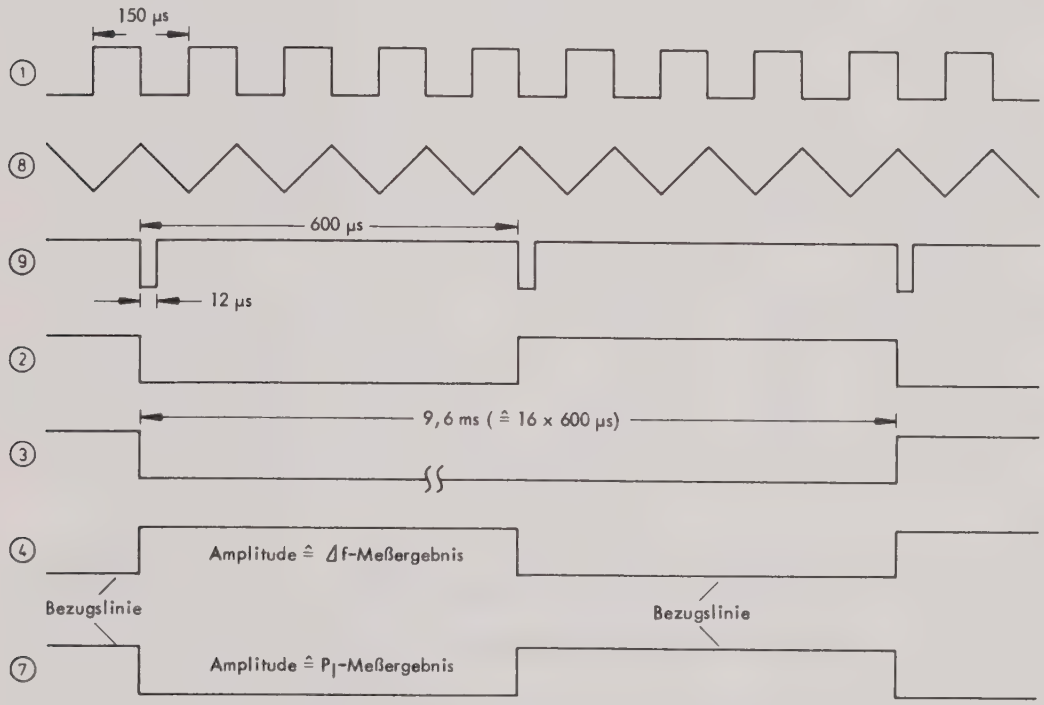


Fig. 10-12a: Impulse plan of X-Y reversing switch

Key for Figure 10-12a:

Messergebnis	=	Test result
Bezugslinie	=	Reference line

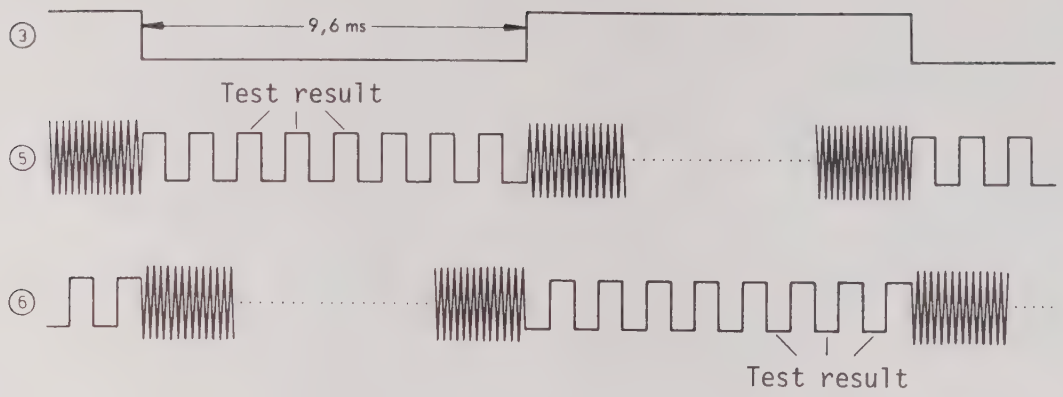


Fig. 10-12b: Impulse plan of X-Y reversing switch (continuation)

In the X-Y reversing switch, either the transistors T 1514, T 1516 or T 1515, T 1517 are switched through. They are controlled by the transistors T 1510, T 1512 and T 1511, T 1513.

The reference line/test result reversing switch in the Y path consists of the transistors T 1508, T 1509. It connects on the one hand the reference voltage, and, on the other, the level result P_I to the input of amplifier IC 1507.

From series E onwards, any deviation from $P_I = 0$ and the reference line can be adjusted with potentiometer 39 (P 1504).

The reference line/test result reversing switch in the X path consists of the transistors T 1507, T 1506. It functions together with IC 1506, in the same way as the reversing switch in the Y path.

The threshhold value switch with IC 1510 is present as an additional special feature. There is a voltage of -150 mV at the minus input of IC 1510. If a test result $<$ 150 mV ($\hat{=}$ 30kHz) reaches the plus input, IC 1510 switchs over T 1521, T 1506 to the reference line. The offset of IC 1506 is adjusted with P 1503.

The X amplifier consists of IC 1509, the Y amplifier of IC 1508. Both are used for amplifying and adjusting the level. At socket Bu 104, they supply a voltage of ±2.5 V, which is taken to the display unit.

The lines to the Display Unit are externally accessible at sockets [54] (socket 302) and [55] (socket 301) at the rear of the Display Unit. By removing the plug-in straps, external units can be connected to the X and Y outputs/inputs.

The section of the circuit containing components T 1524 to T 1530 and IC 1511 to IC 1513 provides improvement of the shape of the frequency markers together with the possibility of charting the frequency markers using the X-Y recorder attachment (26).

The beat-frequency marker is present at Point aM with an amplitude of 4 V_{pp}. This is fed at low resistance via T 1530 to the threshold value switch and limiter formed by T 1528 and T 1529. The output signal from here triggers IC 1512 (retriggerable monoflop). An almost rectangular frequency marker is now produced at the output of monoflop IC 1512 with a notch in the centre of the mark which identifies the correct location of the marker. The frequency markers are superimposed on the measuring results for the X-Y recorder attachment via power sources T 1526 with R 1596 and T 1527 with R 15100.

T 1525 acts as an inverter. T 1524 with R 1590 forms a power source which superimposes the frequency markers on the Y result for the Display Unit via R 1564 or P 1502 and R 1558.

With a 300 Hz bandwidth, the frequency markers are switched off via IC 1501/3.1 by a LOW signal at Point 5 of IC 1512.

IC 1511/2.1 acts as an inverter or as a simple buffer stage depending on whether the signal at Point a1 is HIGH or LOW. This enables the frequency markers to be switched on either during the first half or the second half of the sweep period and thus represented on the calibrating lines or in the result.

IC 1511/2.2 and IC 1513/1.1 suppress the frequency markers if: a1 = LOW (markers on calibrating lines) and bS = HIGH (calibrating lines switched off).

The markers on the calibrating lines have a fixed amplitude. The markers in the measurement results on the display have a variable amplitude (adjustable using P 1502). The markers on the recorder charts have a fixed amplitude.

10.2.16. U_x Generations (16)

In the U_x generation, the deflection signal on the sender side for representing the sweep test result is recovered on the display unit. In the "tracking" mode of operation, the deflection signal appears as a control voltage for the sequential oscillator (8), and is distorted by the characteristic modulation line of the sequential oscillator.

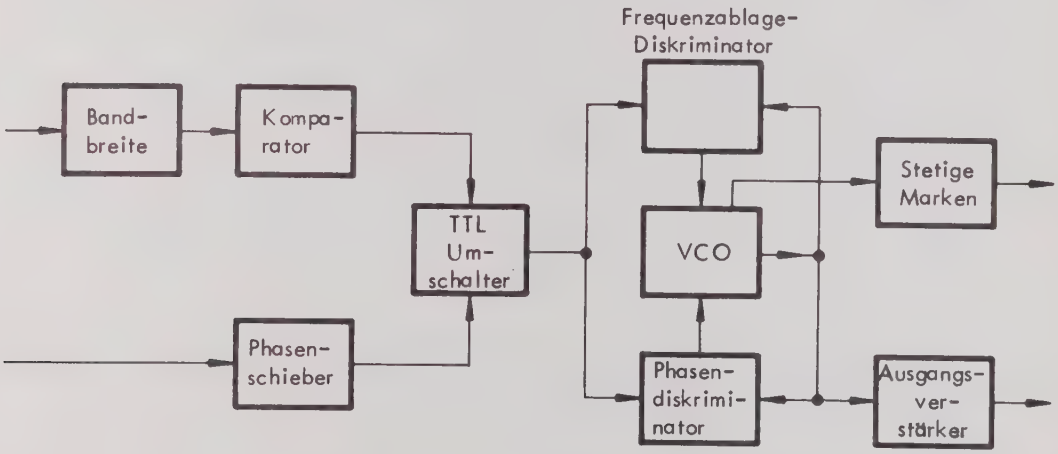


Fig. 10-13: Block circuit diagram of the U_x generation

Key for Fig. 10-13:

Frequenzablage-Diskriminator	=	Frequency indication discriminator
Bandbreite	=	Bandwidth
Komparator	=	Comparator
Stetige Marken	=	Constant markers
TTL Umschalter	=	TTL reversing switch
Phasenschieber	=	Phase shifter
Phasendiskriminator	=	Phase discriminator
Ausgangsverstärker	=	Output amplifier

10.2.16.1. Bandwidth

The control voltage at connection point 9 is limited in the bandwidth to a fixed value of 6 kHz by R 1601, R 1602 and C 1601. The bandwidth of 300 Hz can be connected at point 5 with a LOW signal; it is determined by R 1604, R 1608 and C 1620.

10.2.16.2. Comparator

For crispening the slopes, the comparator with IC 1601 is coupled with C 1607 and R 1610. The offset voltage of IC 1601 is compensated with P 1601.

10.2.16.3. TTL Reversing Switch

The reversing switch consists of IC 1602/4.1 and 4.2 as well as of IC 1603/4.1 and 4.2. IC 1603/4.2 is released with a LOW signal at connection point 6, that is, TTL signals from the comparator can reach the output of IC 1602/4.2.
IC 1603/4.1 is released with a HIGH signal at connection point 6 and TTL signals from the phase shifter can reach the output of IC 1602/4.2.

10.2.16.4. Frequency Indication Discriminator

Negative differentiated impulses with about 3 µs are coming from the input and from the deflection voltage generator IC 1607. The delay time t is about 40 µs.

It is assumed that the input frequency is equal to the generator frequency. The calling key flip-flop IC 1604/4.3 and 4.4 is then alternately set by the input and reset by the generator.

Accordingly however there is a LOW signal at Q, when the next impulse comes from the input and the output of IC 1604/4.1, pin 6 remains at the HIGH signal.

Accordingly, there is a LOW signal at $\overline{Q}$, when the next impulse comes from the generator and the output of IC 1605/3.2, pin 6 remains at the HIGH signal.

The delay t is necessary so that the "first" impulses cannot reach the output.

If the input frequency is greater than the generator frequency, several impulses come from the input before the next impulse comes from the generator.

The first impulse from the input sets the output Q of the calling key flip-flop to a HIGH signal and, after the delay time of t, the IC 1604/4.1 is released for the further LOW impulses until the next impulse comes from the generator.

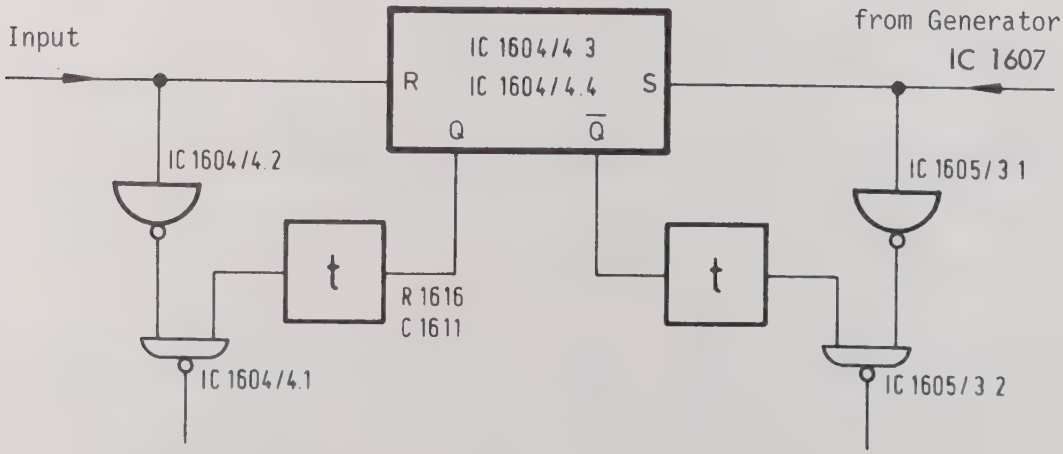


Fig. 10-14: Frequency indication discriminator

In the reverse case, when the generator frequency is greater than the input frequency, the same operation takes place with $\overline{Q}$ and IC 1605/3.2.

If the input frequency is higher, LOW impulses come to the output of IC 1604/4.1. These LOW impulses set the monoflop IC 1606/2.1 so that impulses with a residence time of 5 ms are available at the output of IC 1606/2.1. By means of T 1604 and T 1606, these are converted into current impulses, which are integrated with C 1622 and brought into the regulating circuit over R 1683 in order to retune the generator.

If the generator frequency is too high, LOW impulses appear at the output of IC 1605/3.2 and set the monoflop IC 1602/2.2.

The output impulses are then converted into positive current impulses with T 1603 and T 1605, also integrated with C 1622 and brought into the regulating circuit in order to retune the generator.

In the "Bessel" mode of operation (HIGH signal at connection point 19), the phase regulating circuit is interrupted by connecting T 1611 in the circuit. At the same time, T 1614 is connected in the circuit, thereby placing the control voltage for the Bessel frequency through R 1663, R 1666, P 1607 and over T 1607 at the generator IC 1607.

10.2.16.5 Phase Discriminator

The phase discriminator, consisting of T 1608, C 1619 and IC 1608, operates according to the sample procedure. In the zero passage of the input signal (comparator), a small switching impulse, which puts through the T 1608, is produced. This momentary value of the delta voltage is stored by C 1619 and compared over the voltage follower IC 1608 of IC 1610 with the value set at potentiometer [52] (P 1605).

The deflection voltage generator is adjusted further over T 1612, T 1613 and T 1607.

10.2.16.6 Output Amplifier

The output amplifier IC 1609 makes the sinusoidal signal available at a low resistance. The output voltage is adjusted with P 1603.

10.2.16.7 Phase Shifter

The phase shifter permit the phase of the deflection frequency to be shifted continuously by more than 360^{o} with potentiometer [35] (P 1609).

Two linear ramps are produced with C 1637 and C 1638. The first ramp is started at -12 V with the blocking of T 1615. On reaching 0 V, IC 1613 switchs and starts the second ramp (C 1538) from -12 V. When this also reaches 0 V, IC 1614, whose switching slope is used for the synchronization of the U_x generation, also switches. Frequency independence is achieved by the frequency-dependent control of the power supplies R 1687, T 1621 and R 1690, T 1622. For this, T 1616, IC 1612, T 1617, T 1619 and C 1636 form a frequency discriminator.

10.2.16.8 Constant Markers

For producing two constant markers, the delta voltage of IC 1607 is compared with an adjustable reference [potentiometer 25 (P 1610) or 26 (P 16111)]. The positive switching slope of IC 1616 is differentiated by R 1610, C 1644 and coupled out over T 1626 and T 1628. For the second marker, the positive switching slope of IC 1615 is differentiated through R 1699, C 1643 and coupled out over T 1625 and T 1628. In order to achieve a constant ratio of impulse time to duration of period of the deflection frequency, a frequency-dependent voltage for the differentiating elements is applied over T 1629 and T 1627.

10.2.16.9 Correction Device in the Inout Amplifier

The DC voltage, coming from the demodulator, is compared at connection point 3 and after decoupling by IC 1617, by the level controller with a reference voltage set at P 1612. The difference is amplified with IC 1618 and integrated at C 1647. The level in the input amplifier is re-adjusted with this voltage. In the measuring range, the case may occur however in which the input amplifier has maximum amplification and there is a high level at the input. At the same time, mixer and amplifier are overloaded and produce the second harmonic of the input frequency, on which the frequency regulating circuit rests (the frequency search run commences at high frequencies). In order to prevent this, the monoflop IC i620 is set and changes the charge on IC 1647 in such a manner, that the input amplifier is set briefly on the minimum amplification.

10.2.17. 20 MHz logarithmizer (17)

The 20 MHz logarithmizer is designed for an input frequency of 70 ± 25 MHz and 140 ± 50 MHz. The dynamics of the logarithmizer are 40 dB, so that it is particularly suitable for measurements of the return-loss factor.

The input signal from socket [28] (Bu 1701) is conducted over the buffer stage T 1701 to the mixer IC 1701. The carrier signal for the mixer comes from the sequential oscillator (8) and has a frequency 20 MHz greater than the input signal. The intermediate frequency $f_{IF} = f_T - f_e$ of 20 MHz so obtained is supplied over the amplification stage T 1702, Bu 1704 and Bu 1703 to the amplification stage T 1716. The amplification of the two amplification stages T 1702, T 1716 is approximately 22 dB. The mixed products, produced by the mixer, are suppressed by the 20 MHz band-pass filter which follows. The function of the emitter follower T 1703 is to provide a high-resistance coupling of the cascode stage T 1704 and T 1705 to the 20 MHz band-pass filter.

At the collector of T 1705, the level is regulated to a constant value with the PIN diode Gl 1702. The PIN diode is connected in the circuit parallel to the 20 MHz oscillating circuit L 1704, C 1727, the cathode of the diode being grounded over the 20 MHz series oscillating circuit L 1705, C 1725 and C 1726.

From the collector of the transistor T 1705, the signal path leads over T 1707, T 1708 and the selective amplification stages T 1709 and T 1712 to a peak-value rectifier Gl 1705 and Gl 1706. The rectifier output voltage at the emitter of T 1715 is supplied to the double integrator IC 1705, which compares it with the

reference voltage at R 1786 and changes its output voltage accordingly. By such an action, the transistor T 1713' is more or less energized and its collector current, which flows over Gl 1703 and over the PIN diode Gl 1702, is changed. Because the HF resistance of the PIN diode varies inversely proportional to the DC current flowing through it, the HF level at the PIN diode can be regulated to a constant value by changing the DC current. Therefore, at an higher input level, a greater DC current flows through the PIN diode, which has become low-resistant.

In addition, a larger DC current flows through T 1713 !

The diode law $U_D = U_T \cdot \ln (I_D/I_o)$ is used at this transistor, that is, U_D or U_{BE} is proportional to $\ln (I_D/I_o)$. The base emitter voltage from T 1713' is amplified with IC 1704 and IC 1703 so that a DC voltage change of 80 mV is obtained when there is an input level change of 10 dB at the output of the logarithmizer (connection point 24).

The function of T 1710 is to switch over the band width from 300 Hz to 6 kHz.
The temperature dependence of the base emitter voltage from T 1713' is compensated for with T 1713 (double transistor) and the temperature-dependent slope of the U_{BE} characteristic line is compensated for with R 1749.

In order to achieve a minimum hysteresis of the output signal when the level at the input changes rapidly, the charge on C 1725 and C 1726 is changed by IC 1702 and T 1706 in proportion to the change in the DC voltage at the cathode of Gl 1702.

10.2.18. Preselection (19)

The preselection component is a selective amplifier, whose selection can be switched over for 8 different test frequencies. The output voltage is regulated to a constant level with a correction device.

The test signal comes from connection point 36 to the first amplification stage T 1901, at whose collector one selection circuit (e.g. L 1901, C 1905) is connected at the time in question. The selection circuit is switched over by the diodes Gl 1901 to Gl 1916. On each occasion, two diodes are connected in the circuit simultaneously, e.g. Gl 1901 and Gl 1902 with the corresponding switching transistor (in this case, IC 1903/5.1). Gl 1901 connects the oscillating circuit to the collector of T 1901 and Gl 1902 connects the oscillating circuit with the base of IC 1904/5.4.

The resonance resistance of all oscillating circuits amounts to 1 kΩ, so that an amplification of 12dB results for the amplification stage T 1901. The amplification stages IC 1904/5.4, IC 1904/5.5 and T 1902 also have an amplification of about 12 dB.

The correction device, consisting of T 1904 and T 1905, forms the collector resistance of T 1903 and determines its amplification. The emitter resistance of T 1904 and T 1905 is adjusted at connection point 30 with the adjusting voltage in such a manner, that there is a test voltage of about 7 mV at connection point 31.

The current through the correcting network is proportional to the applied test signal level. A portion of the current is measured with the analog meter I 1901, and is used to indicate when overloading occurs in the 20 dB dynamic range.

10.2.19. Selection (20)

In principle, the design of the selection component is the same as that of the preselection component (19).

The first amplification stage IC 2003/5.1 has an amplification of 6 dB. The second amplification stage T 2001, with the switchable selection circuits as collector resistance, has an amplification of 12 dB. IC 2004/5.5 acts as a buffer stage for the rectifier (21) which follows.

10.2.20. Rectifier (21)

The rectifier consists of a wide-band amplifier, a rectifier, a 6 kHz low-pass filter and a sample-and-hold circuit for the correction device in the preselection.

From the selection (20), the input signal is taken over connection point 125 to the first amplification stage T 2104. The signal is amplified to 2.9 V_{pp} with T 2105 and T 2106. This voltage is rectified with the IC 2104 and amplified by a factor of 11 by IC 2101. The output signal passes over the 6 kHz low-pass filter L 2101, C 2116 and C 2117 and over the connection point 120 to the cross fader (22).

Because the rectified voltage at connection point 120 should be constant, it is amplified by IC 2102 and passed over the FET

switch T 2107 and the source follower T 2109 of the base of the correction device T 1904 into the preselection (19).

On raising the BB level, the recifier output voltage increases. As a consequent, the base voltage at the selection device T 1904 is increased. As a consequence, more collector current flows through the correction device so that its resistance decreases, that is, its amplification becomes less, as does therefore also the rectifier output voltage.

The operating point of the rectifier IC 2104 is adjusted with P 2101 by changing the adjusting voltage for the amplification of the correction device.

So that the $\Delta U/U_o$ result is not leveled by the regulating circuit within a sweep period of, for example, f_A = 70 Hz, the regulating circuit closes for only 50 µs per sweep period. The FET switch T 2107 is closed with a 50 µs impulse and, in this period, changes the charge of the capacitor C 2122. At the same time, the correction device in the preselection (19) is readjusted.

The control impulse is derived from the U_x voltage. The U_x voltage arrives from the U_x generation (16) over connection point 123 at the comparator IC 2103. The 50 µs impulse is produced at the collector of T 2108 from the square-wave voltage at the output of IC 2103 with the differentiating element C 2118 and R 2144. Because the regulating impulse commences in the zero passage of the U_x voltage, and because this corresponds to the center of the image at the display unit of the RME-4, the $\Delta U/U_o$ results are also related to the value of the center of the image.

A square-wave signal, derived from the U_x voltage, is also required for the frequency identification (23). This signal is passed over T 2110 and connection point 121 to the frequency identification (23).

The phase meter (24) receives the test signal over T 2102, whose emitter resistance is provided with a 20 MHz oscillating circuit. The function of the 20 MHz oscillating circuit is to suppress cross-talk voltages from the 20 MHz oscillator in the crystal oscillator component (25). The cross-talk voltage would distort the phase result at the three low test frequencies, because these frequencies are derived from 20 MHz.

10.2.21. $\Delta U/U_o$ Amplifier, $\Delta\varphi$ Amplifier, Cross-Fader (22)

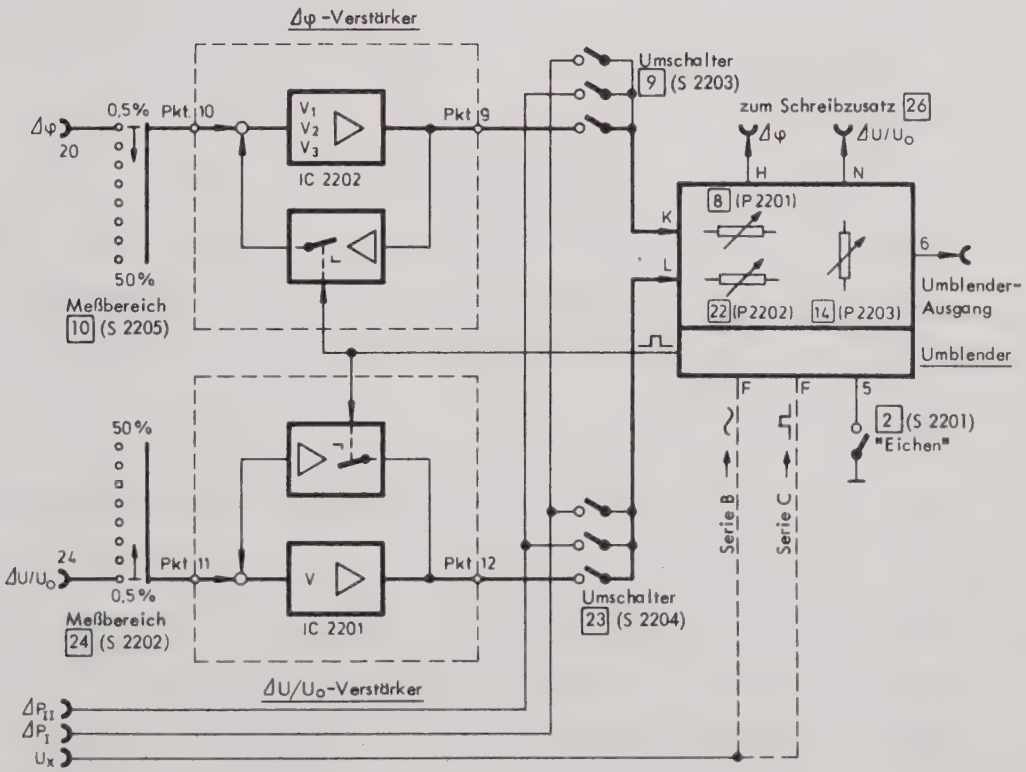


Fig. 10-15 Block circuit diagram of the (22) sub-assembly

Key for Figure 10-15:

Verstärker	=	Amplifier
Umschalter	=	Reversing switch
zum Schreibzusatz [26]	=	To the recording assembly [26]
Messbereich	=	Test range
Umblender-Ausgang	=	Cross-fader output
Umblender	=	Cross-fader
Eichen	=	Calibration

10.2.21.1. $\Delta U/U_o$ Amplifier and $\Delta\varphi$ Amplifier

Both amplifiers are the same except for the additional switching over of the amplification of the $\Delta\varphi$ amplifier. For this reason, only the $\Delta\varphi$ amplifier is described.

The test quantity is carried from the phase meter (24) over the divider [10] (S 2205) into the $\Delta\varphi$ amplifier. By switching on the transistor T 2214 with a 0 V signal at connection point M, the band width can be switched over to 300 Hz (R 2242, C 2205). The output of the $\Delta\varphi$ amplifier is kept DC voltage-free by the coupling capacitor C 2207. The test quantity is in step with the swept frequency (18 to 100 Hz) and is not distorted by the high-pass filter R 2249, C 2207 ($f_g \approx 0.05$ Hz).

When the test frequency is switched over, the phase regulating circuit (24) must be engaged once again. There is a DC voltage jump at the output of the phase meter [24] or the input of the $\Delta\varphi$ amplifier, connection point 10. The capacitor C 2207 must be charged quickly. The FET transistor T 2216 is switched on during 150 µs in step with the swept frequency. The on resistance of the transistor T 2216 is at most 100 Ω. C 2207 is

charged with a high current. It is limited by R 2245.

The U_x signal (square wave at connection point F) is supplied over the transistors T 2234 and T 2222 and limited at the Zener diode Gl 2201 to 5.6 V.

T 2215 normally is connected in the circuit and with this the transistor T 2216 blocks. T 2215 is blocked with the negative slope of the square-wave signal. The charge on the capacitor C 2206 is reversed by R 2224 until the transistor T 2215 is again connected in the circuit.

The amplification of the $\Delta\varphi$ amplifier, which depends on the test frequency, is switched over with transistors T 2217 and T 2219. The corresponding TTL switching signal is carried over connection points 7 or 8.

Meßfrequenz	Verstärkung	T 2217	T 2219
92,6 kHz	8,3	aus	aus
83,3 kHz	9,2	aus	aus
555 kHz/277 kHz	13,8	ein	ein
500 kHz/250 kHz	15,3	ein	ein
>1 MHz	9,6	ein	aus

Table 10-2: Test frequency-dependent switching over of the amplification of the $\Delta\varphi$ amplifier

Key for Table 10-2:

Messfrequenz	=	Test frequency
Verstärkung	=	Amplification
aus	=	Off
ein	=	On

The amplification data in Table 10-2 is valid between connection points 10 and 9. The amplification of the $\Delta U/U_o$ amplifier between connection points 11 and 12 is 11-fold.

.2.21.2. Cross Fader

With the help of the cross-fader, a maximum of 3 signals can be represented simultaneously on the CRT screen:

- The test signals at the cross-fader input I and II in chopper operation with 16 kHz in the beam return
- A calibrating square wave with 16 kHz in the beam advance

A 16 kHz oscillator, which consists of T 2221 and T 2223, functions as a source for producing the chopper frequency and the calibrating square wave.

The pulse duty factor of the chopper frequency at the collector of T 2224 can be changed in the pulse duty factor converter. By so doing, a longer "on" time period of 1 test trace relative to the others can be obtained. In the final analysis, this becomes noticeable as a brightness change on the CRT screen (see Figure 10/16).

At Pin 5 of IC 2204/5.5, there is a delta voltage, whose symmetry

is adjustable with P 2207. By altering the DC voltage, superimposed on the delta voltage, with potentiometer [14] (P 2203), the trigger onset of the following Schmitt trigger IC 2208/5.1, IC 2208/5.3 and therefore also the pulse duty factor of the output voltage are altered.

The output voltage acts as on the differential amplifier IC 2209/3.1, IC 2209/3.3. T 2228 or T 2229 becomes conducting, depending on which branch of the amplifier is carrying current: that is, the path for the signal from cross-fader input I or cross-fader input II, to the inverter IC 2210 becomes free.

The 16 kHz frequency passes over the slope crispener T 2224 and simultaneously reaches the calibration limiter IC 2204/5.2 and T 2226. The power supply of the limiter IC 2204/5.3 is temperature compensated and largely stabilized against fluctuations in the operating voltage.

The lower trace of the calibration square wave ($\hat{=}$ - 200 mV) is determined by a current, which comes from the current distribution point R 2295 and can be adjusted with P 2204. The upper trace of the calibration square wave ($\hat{=}$ + 200 mV) is determined by a current, which flows to the resistance R 2295 and can be adjusted with P 2205.

The calibration square wave reaches T 2227 directly and from there is conducted over the inverter IC 2210 to the cross-fader ouput.

The release of the calibration square wave to the output depends on the U_x (switching) signal and is accomplished through IC 2208/5.5.

If switch [2] (S 2201) is closed the U_x signal from connection point F passes over T 2234 and T 2225 to the transistor IC 2208/5.4.

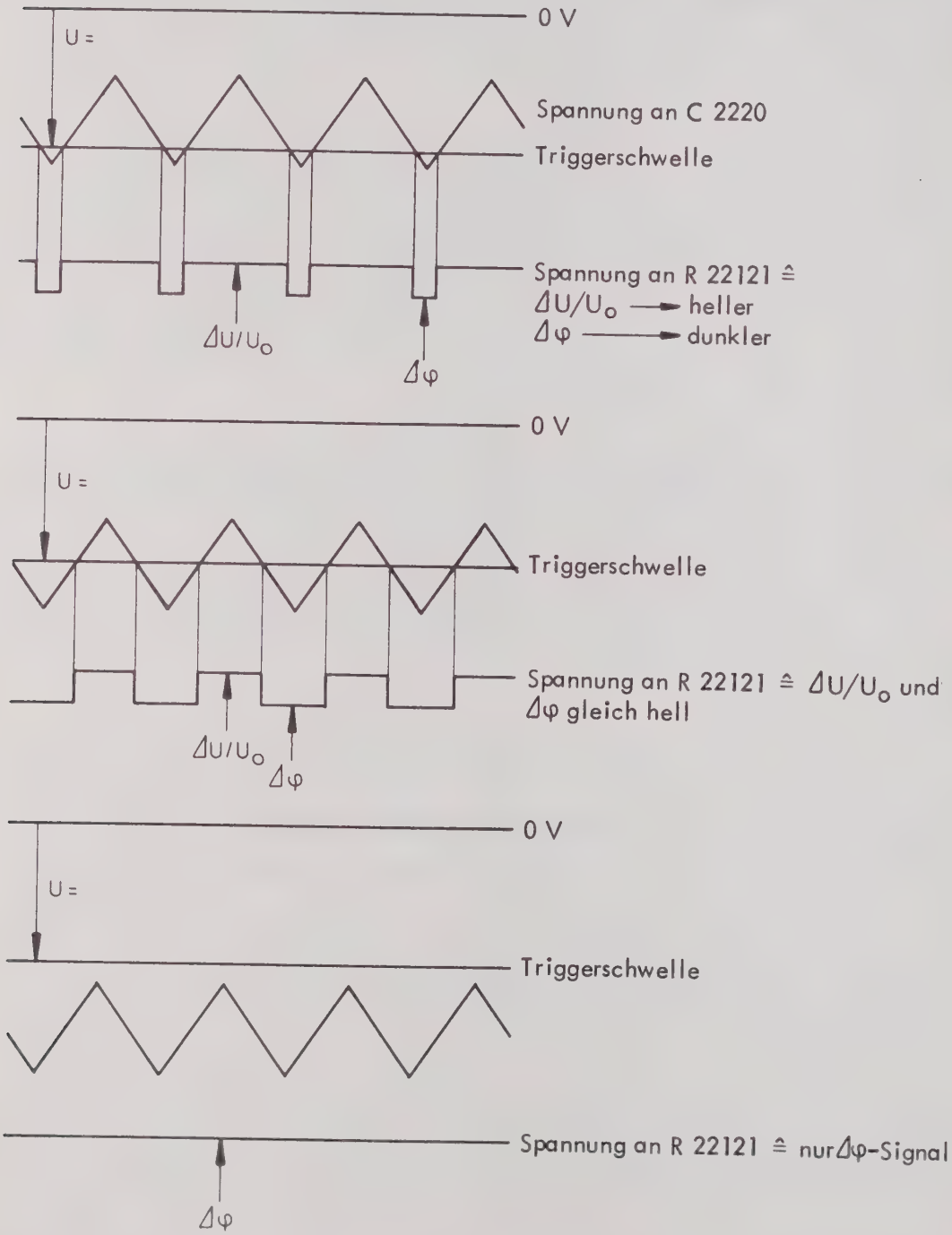


Fig. 10-16
Brightness change of the test results shown, as a consequence of a pulse duty factor change of the chopper frequency

Key for Figure 10-16:

Spannung an	=	Voltage at
Triggerschwelle	=	Trigger threshhold
heller	=	brighter
dunkler	=	darker
und	=	and
gleich hell	=	Equally bright
nur $\Delta\varphi$ signal	=	$\Delta\varphi$ signal only

When this is conducting, current is withdrawn from the differential amplifier IC 2209/3.1, IC 2209/3.3 over Gl 2221 and Gl 2222.

The consequences of this are that the gate connections of T 2228 and T 2229 become negative; the signal paths from the cross-fader input I and II are blocked. If transistor IC 2208/5.4 is conductive, IC 2208/5.5 blocks. With this, T 2227 is conductive, releasing the signal path for the calibration square wave.

With potentiometer [8] (P 2201) and [22] (P 2202), the starting points of the test traces can be displaced in the Y direction beyond the boundaries of the calibration square wave.

With potentiometers P 2206 and P 2208 at connection point H and N, the zero lines for the recorder accessory (26) are adjusted to -200 mV.

.2.21.3. Y_{ext} Input

At the back of the instrument, it is possible to feed in a signal to the RME-4 over input [53] (Bu 2201). The input is DC voltage-coupled and has a sensitivity of 1 mV/graticule division. The

signal supplied can be displayed on the CRT screen by pressing the two push buttons ΔP_{II} and $\Delta\varphi$ or ΔP_{II} and $\Delta U/U_o$ simultaneously. The externally supplied signal can be recorded if the RME-4 is euqipped with a recorder assembly.

The externally supplied signal passes from input [53] (Bu 2201) over connection point 53 to the IC 2203, with which the signal is amplified by 32 dB and supplied over R 22165 and R 22166 to the keyboard rows [9] (S 2203) or [23] (S 2204). From these push buttons onwards, the signal is processed further just like all other signals at the keyboards rows.

10.2.22. Frequency Identification (23)

This component identifies the frequency of the BB voltage and then turns on the appropriate selection circuits in the preselection (19) and selection (20). In addition, the amplification in the phase regulating circuit (24) is switched over and the appropriate test frequencies in the crystal oscillator (25) are turned on.

The BB signal passes from connection point (19) 36 over the emitter follower T 2308 to the first amplification stage T 2301 of the frequency identification. The level is controlled at TP 2301 to a constant value with the variable-gain amplifier IC 2301 which follows and which has a dynamics of at least 20 dB. The voltage at TP 2301 is rectified with the rectifier IC 2303 and its DC voltage is compared with the voltage at pin 2 of IC 2302. Depending on the difference between the two voltages, the amplification of IC 2301 is adjusted with the output voltage of IC 2302. The voltage at

TP 2301 is adjusted with P 2301 to 0.7 V_p. The two diodes Gl 2317 and Gl 2318 limit the interfering voltages which arise in the case of IF tracking operation. In this connection, it is a question of mixed products with frequencies f ≦ 32 MHz.

The spurious traces f = 2 f_Z - f_T and f = 3 f_Z - f_T (f_Z = character frequency, f_T = carrier frequency) are particularly bothersome.

From TP 2301, the BB signal passes over the emitter follower T 2303 and reaches the 8 series oscillator circuits, which are connected parallel. A rectifier is connected to each oscillator circuit coil..

If, for example, the BB signal has a frequency of f = 5.6 MHz, the oscillator circuit addresses C 2332, L 2305. C 2332 is charged over Gl 2309 by the resonance step-up and T 2306 cuts into the circuit. In the wiring of the BB path sub-assembly (29), the "C" signal passes over connection point 57 and reaches IC 2902/6.1. The frequency position in the preselection (19), selection (20), crystal oscillator (25) and phase regulating circuit (24) are energized with IC 2902/6.1, IC 2902/6.2 and IC 2904/5.4.

During the negative half-wave of the U_x voltage, T 2303 is blocked with T 2304, so that several frequency positions cannot be connected in the circuit simultaneously, as would be possible in IF operation because of the spurious traces. In terms of frequency, the negative path wave of the U_x voltage corresponds to the frequency range below the center frequency which has been set at the RMS-4. The control voltage for T 2304 is a square-wave voltage, which is derived in the rectifier (21) from the U_x voltage.

10.2.23. Phase Meter and Phase Regulating Circuit (24)

The sinusoidal voltage from the test signal input, connection point 63, is limited by IC 2405 and lies as a square-wave voltage at the input of IC 2407/2.2. A square-wave voltage from the crystal oscillator of the same frequency but with a displaced frequency, lies at the input of IC 2407/2.1. The frequency of both signals is divided to half the value by IC 2407.

IC 2406 is an exclusive OR, which indicates the phase difference between TP 2402 and TP 2403 by a specific pulse duty factor (Figure 10-17). The function of the low-pass filter between IC 2405 and IC 2407 is to attenuate the pulse spikes.

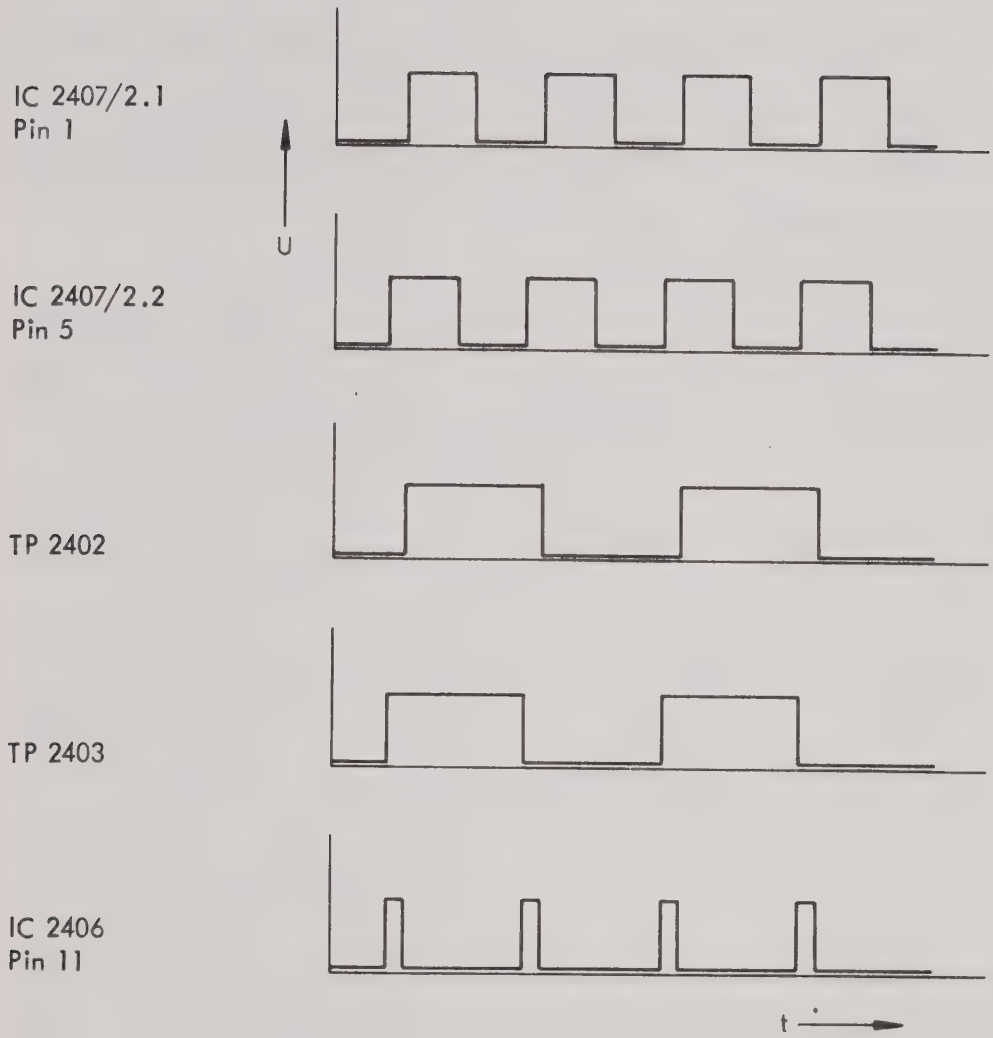


Fig. 10-17: Impulse plan of the phase meter

The function of the following differential amplifier T 2410, T 2412 is to crispen the slopes and to limit.

The low-pass filter L 2401, C 2412, C 2414 at the output of the differential amplifier integrates the voltage.

IF the difference between the frequencies at the inputs (connection points 62 and 63) is only a few Hz, the phase transit is continuous and therefore the voltage behavior at the output of the low-pass filter is as shown in Figure 10-18.

The phase result after the low-pass filter is amplified through T 2414 and IC 2408 by the factor of 10 and is passed over the $\Delta\varphi$ amplifier and the cross-fader (22) to the display.

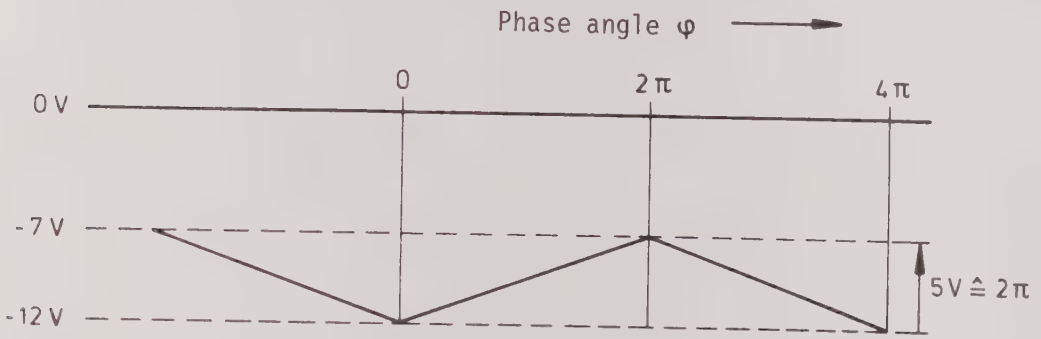


Fig. 10-18: Voltage at the output of the low-pass filter

The low-pass filter of C 2415 and R 2457, to which the voltage 0 V ± ΔU is offered, has a cut-off frequency of 6 kHz, as does the previously described low-pass filter. Both low-pass filters are intended to prevent the test frequency (e.g. 92 kHz) being displayed. The high-pass filter of C 2416 and R 2461 is intended

to prevent amplification of the DC voltage.

The phase result at the collector of T 2410 is supplied over T 2409 to the phase regulating circuit. The $\Delta\varphi$ result is attenuated by 46 dB by means of R 2433, and R 2432; the absolute value of the $\Delta\varphi$ result is integrated with C 2404 and amplified by the amplifier from T 2404', T 2404, T 2402 and T 2401. The resistances for f_M = 2.4 MHz, which determines the amplification, are R2408 and R 2418 Depending on which test frequency is selected, the appropriate FET switch IC 2401 or IC 2403 connects the corresponding resistance, which determines the amplification, into the signal path. The crystal oscillator (25) is readjusted with the output voltage at connection point 79 to the test frequency, which the phase meter (24) receives from the rectifier (21). Accordingly, the two frequencies at connection points 62 and 63 are in phase, and rapid phase changes of the test frequency relative to the oscillator comparator frequency are indicated by the phase meter.

0.2.24. Crystal Oscillator (25)

The crystal oscillator is a part of the phase regulating circuit and supplies the reference signalagainst which phase variations are measured. It must therefore produce the same frequencies, which the RME-4 receives as test freqencies from the RMS-4. In every case, it must be possible to regulate the frequency uncertainty of the RMS-4 ($2 \cdot 10^{-5}$) with the help of the regulating circuit. As a special property, the oscillator has a very good short-term stability.

The signal with 20 MHz at connection point 115 is used in the following components:

- in the auxiliary regulating circuit as reference
- divided into 200 kHz, as a reference in the display and deviation measurement rectifier
- for the generation of frequency markers.

The 20 MHz oscillator and the oscillator for producing test frequencies >1 MHz are similarly constructed. It is a transistor-degenerative oscillator (T 2502, T 2503 or T 2505, T 2506), whose frequency-determining element is the crystal in the emitter circuit. With the help of a capacitance diode, the frequency of the oscillators can be varied by about $2.5 \cdot 10^{-4}$ over a common control lead (connection point 109). The highest frequency of the test frequencies >1 MHz is adjusted to the nominal value with T 2501 at U = 0 V (connection point 109). This is necessary because the least controlling voltage is available to the phase control at high frequencies. However, so that the tolerances for the control voltage also remain small at other test frequencies > 1 MHz, a diode quartette was used for the capacitance diodes (with the exception of Gl 2519 for f_M = 2.4 MHz). A common capacitance diode for the test frequencies > 1 MHz is therefore impossible, because the capacitive load would become too great and the crystals could no longer be pulled after high frequencies.

The emitter phase T 2504 or T 2512 converts the oscillator amplitude into TTL voltages.

The T 2504 stage supplies the 20 MHz output and IC 2501. Depending on the test frequencies series to be produced (Series I = 92.593 kHz; 277.778 kHz; 555.556 kHz or Series II = 83.3 kHz; 250 kHz; 500 kHz), the 20 MHz oscillator frequency is divided by 9 or 10, which can be accomplished easily by changing the soldering connections of the solder straps. The 4:1 divider IC 2502 produces 555.5 or 500 kHz, a further 2:1 divider IC 2503 produces 277.7 or 250 kHz and the additional 3:1 divider IC 2503 produces 92.593 or 83.3 kHz. The frequencies are switched to the output, connection point 103, over the gates IC 2505 and IC 2504. If none of the three test frequencies < 1 MHz are connected in the circuit, the gates IC 2505/4.3 IC 2505/4.4 and IC 2504/4.2 are cut out of the circuit and, in addition, the 9:1 or the 10:1 divider IC 2501 is blocked over the diodes Gl 2507, Gl 2506 and Gl 2505, so that no beat frequencies can arise with the test frequencies > 1 MHz.

Each test frequency > 1 MHz (2.4; 5.6; 8.2; 12.39 MHz and a color subcarrier frequency) has its own crystal. For example, with the help of the PIN diode Gl 2510 and the switching stage T 2507, the Q 2502 crystal is connected to the T 2506 emitter, while all other crystals are disconnected over PIN diodes. The transistor stage T 2514 produces the bias voltage for the PIN diode. In the case of an H signal at A, T 2507 is conductive and a current can flow through the PIN diode; in the case of an L signal at A, T 2507 is blocked and the PIN diode is blocked with $\sim$6V. The Q 2502 crystal is now disconnected from emitter T 2506 by a high resistance. The mode of operation for the other four crystal positions is similar.

In order to be able to allow the oscillator to oscillate in a relatively small frequency range, the frequencies of the crystals were selected so that their frequency provides the use frequency when divided by 1, 2 or 4. The reason for this measure is the absence of selection by the oscillator.

The division factors were connected in the circuit in the following matter:

Crystal Frequency		Use Frequency
12.39 MHz:1	=	12.39 MHz
8.2 MHz:1	=	8.2 MHz
11.2 MHz:2	=	5.6 MHz
f_{sc} [1]:2	=	f_{sc} [1]
9.6 MHz:4	=	2.4 MHz

By interconnecting the diodes Gl 2522 to Gl 2530 differently, other division factors and therefore also other frequencies can, within certain limits,be assigned to the frequency positions.

The division of the oscillator frequency by 2 and 4 is accomplished by IC 2506 and the distribution to the output goes over the gates IC 2504/4.3, IC 2504/4.4 and the transistor stage T 2513.

The instructions to trigger the individual frequencies come from the frequency identification sub-assembly (23) over the wiring of the BB part (29) , the L signals being required for

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1)sc = subcarrier =color carrier frequency

connecting the test frequencies < 1 MHz in the circuit and the H signals for connecting the test frequencies > 1 MHz.

10.2.25. Recorder Assembly (26) (Additional Equipment, Present only if Requested)

The circuit can be divided into the various functional groups, which are described in greater detail in the following.

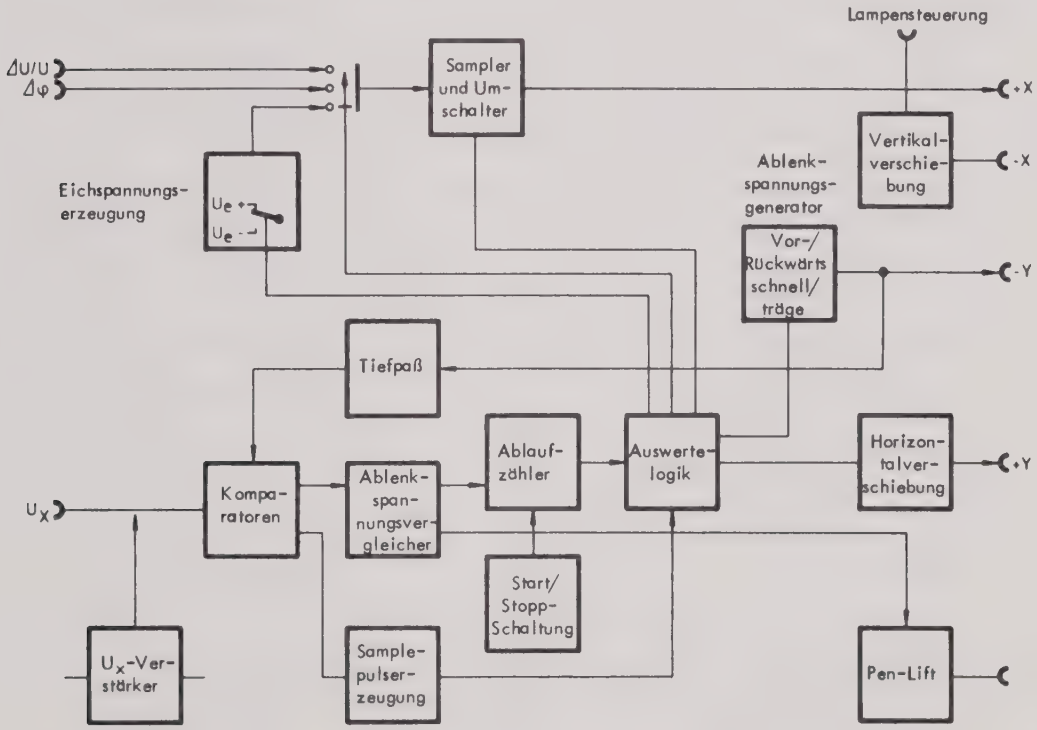


Figure 10-19 Block Circuit Diagram of the Recording Assembly

Key for Figure 10-19

Sampler und Umschalter	=	Sampler and Reversing Switch
Lampensteuerung	=	Lamp control
Eichspannungserzeugung	=	Calibration voltage generation
Ablenkspannungsgenerator	=	Swept voltage generator
Vertikalverschiebung	=	Vertical displacement
Vor-/Rückwärts schnell/ träge	=	Forwards/backwards, rapidly, slow
Tiefpass	=	Low-pass filter
Komparatoren	=	Comparators
Ablenkspannungsver- gleicher	=	Swept voltage comparator
Ablaufzähler	=	Process counter
Auswertelogik	=	Scoring logic
Horizontalverschiebung	=	Horizontal displacement
U_x-Verstärker	=	U_x Amplifier
Samplepulserzeugung	=	Sample pulse generation
Start/Stopp-Schaltung	=	Start/Stop circuit
Pen-Lift	=	Pen-Lift

10.2.25.1.Control

Comparators

The scanning of the test results is based on the sample principle. A slow swept voltage is compared in amplitude with the rapid U_x voltage. If the two voltages are the same, a pulse is produced which closes a switch. Over this switch, a capacitor is charged to the test value present.

In the comparator circuit, the information is obtained which is required for producing the sample pulses and for controlling the process.

The three comparators IC 2602, IC 2603 and IC 2604 receive the U_x voltage over a buffer amplifier IC 2601.

Sample Pulse Generation

The circuit should operate with very different swept frequencies (18 to 100 Hz). The ratio of the duration of the sample pulse to the duration of the period should be independent of the swept frequency. This requirement is fulfilled by the circuit used. In addition the advance or return information is obtained directly with this circuit.

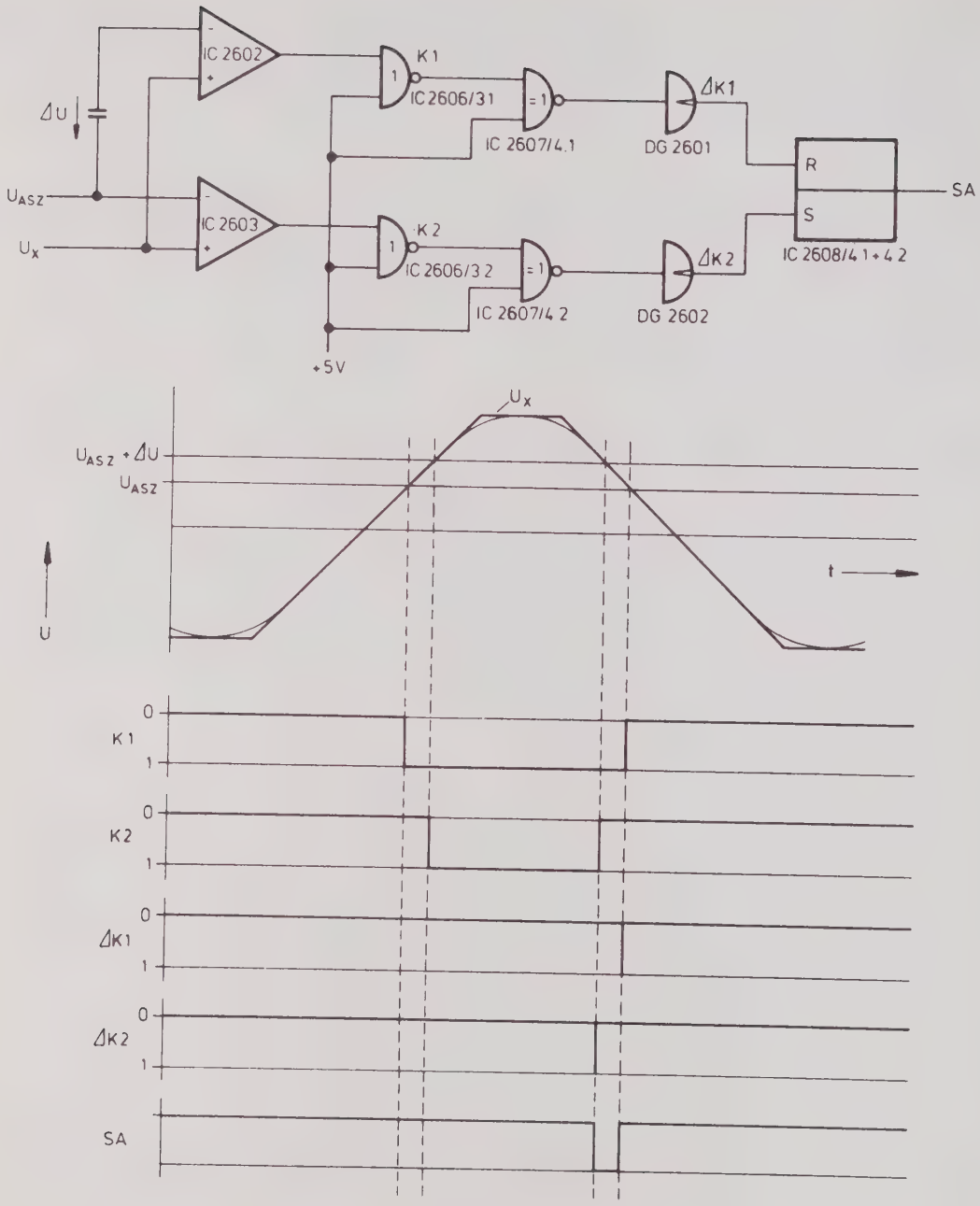


Figure 10-20 Schematic Circuit Diagram and Impulse Plan of the Sample Generation

The sample pulse SA is processed further in the scoring logic.

Figure 10-20 shows the schematic circuit diagram and the impulse

plan of the sample pulse generation.

Swept Voltage Comparator

This part of the circuit determines whether $|U_{ASZ}| \leqq |U_x|$, that is, whether a test result is present (see Figures 10-21 and 10-22).

For this purpose, comparators IC 2603 and IC 2604 are used, while IC 2604 determines the zero passages of U_x. IC 2603 switches at the times of scanning.

At the start, the swept voltage U_{ASZ} of the recording assembly is more negative than the swept voltage U_x. At the control input, pin 2, of the exclusive OR gate IC 2607/4.3, which is used here together with IC 2607/4.4 as "polarity reverser", there is a 1 signal, that is, $K2^x = K2$ and $K3^x = K3$. After the start instruction, the swept voltage U_{ASZ} commences to rise in the positive direction. When U_{ASZ} and U_x are equal for the first time, the RS flip-flop IC 2610/3.2 and 3.3 is reset over gate IC 2610/3.1 by the $K2^x = 0$ signal.

The RS flip-flop IC 2609/4.1 and 4.2 is in each case set by $\Delta 1 = 1$ signal and reset by the $K2^x = 1$ signal. Its output voltage prevents over gate IC 2610/3.1 the setting of the RS flip-flop IC 2610/3.2 and 3.3. Only in the absence of the $K2^x = 1$ signal, that is, when $|U_{ASZ}|$ has become greater than U_x, does the RS flip flop IC 2609/4.1 and 4.2 remain set. As a result, the path over gate IC 2609/4.4 is free for $\Delta 2$ and the RS flip-flop IC 2610/3.2 and 3.3 is set.

By so doing, the JK flip flop IC 2613/2.1 is switched, which stores the information "advance ended". The circuit is prepared for the reverse traverse with the output signal of the JK flip-flop IC 2613/2.1 ($K2^x = \overline{K2}$ and $K3^x = \overline{K3}$).

Over a blocking line to IC 2610/3.1, the circuit is prevented by the monoflop IC 2612/2.2 from being set by spurious spikes while switching over.

As a result of the switching over of the exclusive OR gate, the relationships during the reverse traverse are the same as during the advance. At the end, the JK flip-flop IC 2613/2.1 is switched back, and the initial state is again attained.

The output signal of the circuit (signal (1)) is used for controlling the pen lift and the cycle counter.

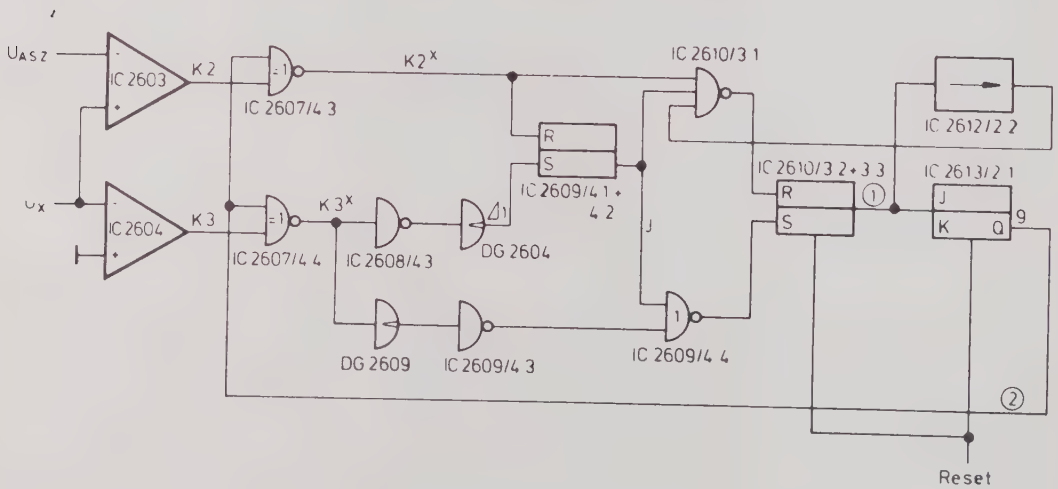


Figure 10-21 Schematic Circuit Diagram of the Swept Voltage Comparator

Cycle Counter

The cycle counter consists of several JK flip-flops, which store the information in regard to which program step is being processe

Two monoflops determine the delay times between the program steps.

Cycle Plan

The temporal sequence of the signals is evident from the cycle plan in Figure 10-24.

Delay Times

Monoflop IC 2612/2.1 has a down-time of 100 ms. It blocks the switching over of the vertical output voltage until it has been made certain that the pen lift has been lifted (signal (7)).

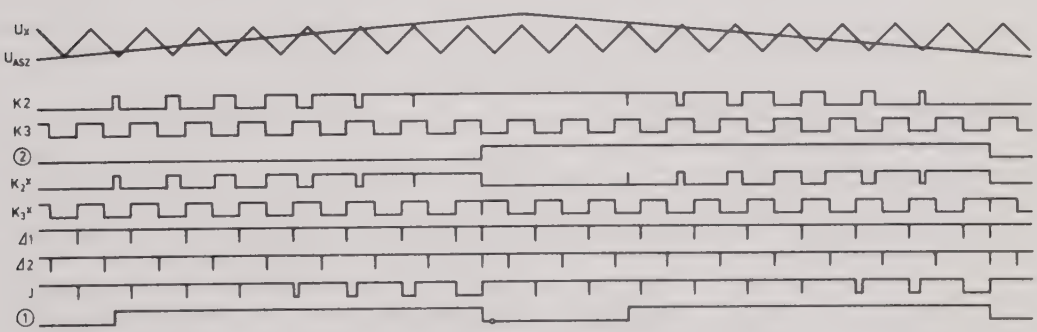


Figure 10-22 Impulse Plan of the Swept Voltage Comparator

Monoflop IC 1612/2.2 has a down-time of 900 ms. The cycle is delayed by the monoflop until the storage capacitor has been charged to the initial value of the test result.

Both monoflops are actuated by the signals (1) and (5), which show that the recording process has been concluded.

JK Flip-Flop

IC 2613/2.1, Pin 9 stores the advance/reverse traverse (signal (2))
IC 2613/2.2, Pin 12 stores the first field/second field (signal (3))
IC 2614/2.1, Pin 9 stores the $\Delta\varphi$ result/$\Delta U/U_o$ result (signal (4))
IC 2614/2.2, Pin 13 stores the start instruction, that is, it remains set until the program is ended or terminated by activating the stop push button (signal (6)).

Scoring Logic

With the help of the scoring logic, the control signals for the analog portion are obtained from the output signals of the cycle counter. The logic relationships are evident from the cycle plan (Figure 10-24) and the circuit diagram in the appendix.

Start-Stop Device

Start Push Button

The recording process is actuated over a microswitch [19] (S 2601). In order to counteract the chatter of the switch a RS flip-flop IC 2611/4.1 and 4.2 follows.

Turning On, Stopping

When push button [19] (S 2601) is depressed, the flip-flops IC 2610/3.2 and 3.3, IC 2613/2.1, IC 2613/2.2 and IC 2614/2.1 are

reset. When the push button is released, the JK flip-flop IC 2614/2.2 is set. By so doing, the instruction "RS" (rapid reverse traverse) is erased, which is switched on during the pause, as is the instruction "V" (advance). Since the signal now is "V" = 1 signal, the program commences. If the push button is activated while the program is running, the flip-flops IC 2610/3.2 and 3.3, IC 2613/2.1, IC 2613/2.2 and IC 2614/2.1 are reset as the push button is pressed. On releasing the push button, the JK flip-flop IC 2614/2.2 is reset and the system once again is inoperative.

If the program is not stopped, the JK flip-flop IC 2614/2.2 is reset after the right image is traced. (④ then makes a negative jump).

10.2.25.2. Obtaining the Test Result and Calibration Voltage

Production of the Calibration Voltage

Between 0 and -400 mV, the calibration voltage is switched over to IC 2613/2.2, Pin 12, by T 2614 with the signal "upper calibration". The calibration voltage is adjusted accurately with P 2605.

Sampler and Reversing Switch

The calibration voltage and the two test results are applied over the collector stage T 2615, T 2616, T 2617, the electronic switches T 2618, T 2619, T 2621 and the resistance R 2698 to the charging capacitor C 2637.

With the signal "calibration", the calibration voltage is switched over G1 2619 through to IC 2611/4.4; the test results are switched through with the sample pulses "SA 1" to IC 2617/3.3 over C 2634 or with "SA 2" to IC 2617/3.2 over C 2635.

The voltage of the charging capacitor C 2637 passes over a FET drain stage T 2623 and a DC voltage amplifier IC 2622 to the recorder input +X. The offset of the circuit is compensated for with P 2606.

Vertical Shift

The vertical shift is accomplished by changing the voltage at the -X input of the recorder. In the BB part, the test frequency received is identified and an appropriate logic signal is obtained. By so doing, a resistive divider is connected in the circuit of component (14) and a DC voltage is produced, which corresponds to the test frequency.

10.2.25.3.Swept Voltage Generation

Swept Voltage Generator

The swept voltage generator consists of three electronically switchable power supplies, which supply an integrator.

With the FET drain stage T 2609, the discharging current of the capacitor over the preconduction current of the amplifier becomes neglegible relative to the currents from the power supplies.

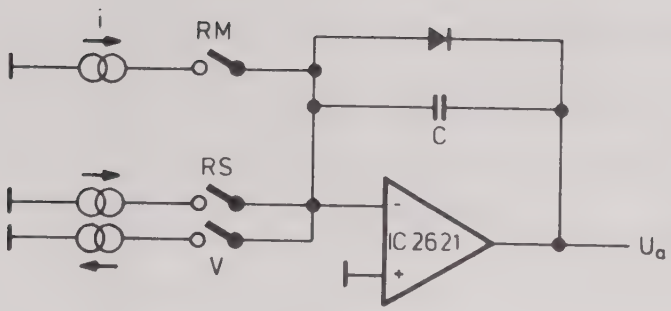


Figure 10-23 Schematic Circuit Diagram of the Swept Voltage Generator

The following relationship holds: $\frac{dU_a}{dt} = \frac{i}{C}$

Because i and C are constant, U_a changes as a function of time. In the position of rest, RS and V are connected in the circuit. The current $i_{RS}-i_V$ flows over the diode G1 2620 after the capacitor is discharged. The voltage at connection point c is adjusted with P 2604 (-2.6 V). The function of the power supplies is evident from the circuit diagram. The recording time is set with potentiometer P 2603 (2/20 s).

The output voltage of the generator is applied to the Y input of the recorder over a 2:1 divider.

Low-pass Filter

In the low-pass filter R 2665, C 2631, the time response of the recorder is simulated. As a result, there is a voltage at the comparators which, independently of the rate of change, corresponds to the geometric position of the pen. The low-pass filter is balanced when the horizontal displacement of the calibration line from the test line disappears.

Horizontal Displacement

Switching over from the right to the left image is accomplished by signal (4) at IC 2614/2.1 Pin 9 over T 2612. At the same time, the voltage at the +Y input of the recorder is switched from 0 V to +3.3 V.

10.2.25.4. Pen Lift

The pen lift of the X-Y recorder is activated over the REL 2601 relay. In the recording position, the normally open contact of the REL 2601 relay is closed.

The voltage, when the relay is switched off, is limited by the diode Gl 2633, which is parallel to the relay coil.

10.2.25.5. Calibration Level Generation at the Right Edge of the Image

The U_x voltage of 4 V_{pp} is at the output of IC 2601. This voltage is rectified with the rectifier (consisting of IC 2624, Gl 2637 and the charging capacitor C 2644) and is available at the output of IC 2625 with $Z_{out} = 0$. At the time of scanning ($\overline{jump}$ = HIGH and $U_{integr.} > 0$ V), T 2625 is switched inversely (low residual voltage). The window comparator IC 2602, IC 2603 then switches at the potential, which is specified by the rectifier and, with the sample pulses derived from this potential, scans the test result at the U_x voltage value

$$U_X \cdot \frac{100\ k\Omega}{100\ k\Omega + 2.2\ k\Omega}$$

that is, the initial value of the test result practically lies at the edge of the curve under consideration.

R 26119 prevents switching of T 2626 when $U_{integr.} < 0$ V (necessary, because the switching variable $\overline{JUMP}$ assumes the value H even when $U_{integr.} \approx -2$ V and the test result does not have to be scanned at this value).

The two diodes Gl 2635 and Gl 2636 are required to switch T 2626 because the HIGH level of $\overline{jump}$ can amount to at least 2.4 V (emitter potential 3.1 V - 2.4 V = 0.7 V > 2 · U_{Diode}).

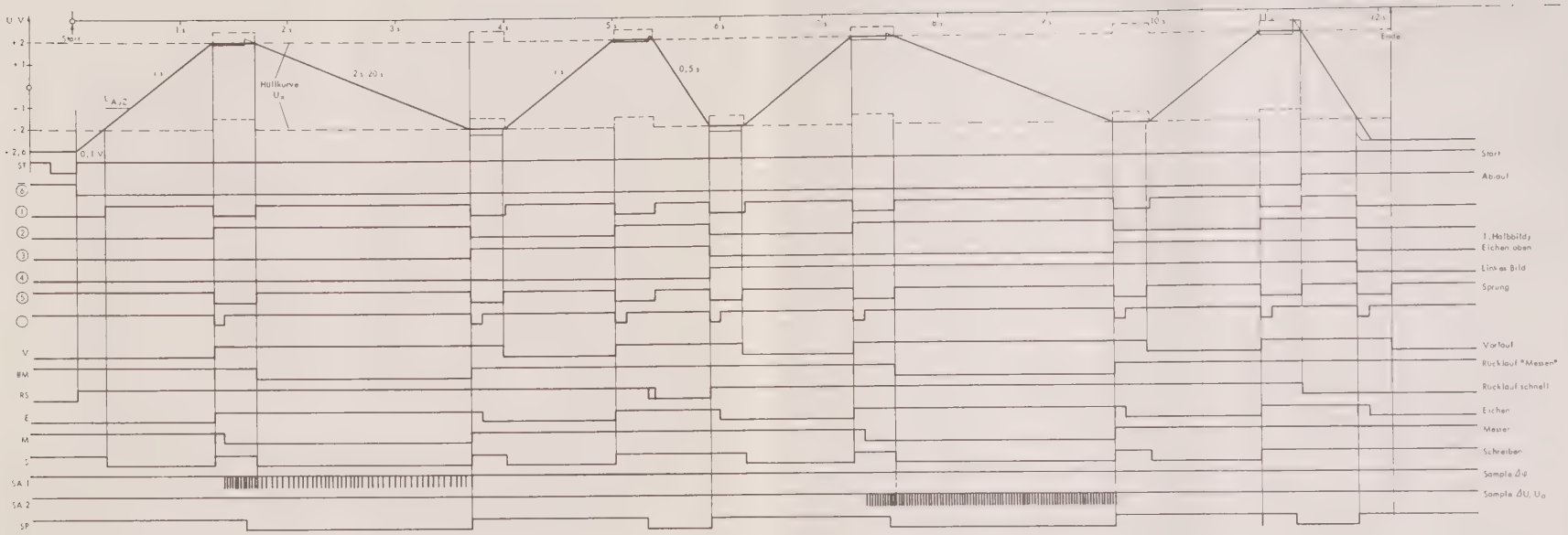
10.2.25.6. List of Control Signals in the Recording Assembly and Cycle Plan Sub-assembly

Signal Description	Test Point	Functional Group in the Block Circuit Diagram (Figure 10-19)	1 Signal Signifies
①	IC 2610/3.2 pin 6	Swept voltage comparator	$\|U_{ASZ}\| > \|U_x\|$
②	IC 2613/2.1 pin 9	Cycle counter	Advance phase
③	IC 2613/2.2 pin 12	Cycle counter	First field; calibration at top
④	IC 2614/2.1 pin 9	Cycle Counter	Left image
⑤	IC 2612/2.2 pin 5	Cycle counter	Waiting time until the charging capacitor is charged to the initial value
⑦	IC 1612/2.2 pin 7	Cycle counter	Waiting time until the pen has lifted off

Signal Description	Test Point	Functional Group in the Block Circuit Diagram (Figure 10-19)	1-Signal Signifies
(6)	TP 2605	Start/Stop Circuit	Cycle: Recording assembly in operation
		Swept voltage comparator	See Section 10.2.25.1.
E	IC 2611/4.4 pin 6	Scoring logic	Calibration voltage at the charging capacitor
K1 K2 K3	TP 2601 TP 2602 TP 2603	Comparators	Output voltage of the Comparators
$K2^x$ $K3^x$	IC 2607/4.3 pin 3 IC 2607/4.4 pin 6	Swept voltage comparator	K 2, K 3 after polarity inverter
M	IC 2617/3.1 pin 12	Scoring logic	"Measuring": The path for scanning is switched through
$\overline{RM}$	IC 2615/4.4 pin 13	Scoring logic	Reverse traverse "measuring": The reverse traverse is switched to slow (2/20 s)
$\overline{RS}$	IC 2616/4.3 pin 1	Scoring logic	Rapid reverse traverse: Reverse traverse is switched to 0.5s
$\overline{S}$	IC 2616/4.4 pin 13	Scoring logic	Pen down: The recorder is operating
$\overline{SA}$	TP 2604	Sample pulse generation	Scanning impulses
SA 1 SA 2	IC 2617/3.3 pin 6 IC 2617/3.2 pin 8	Scoring logic	Scanning pulses $\frac{\Delta\varphi}{\Delta U/U_Q}$
SP	(27)	Scoring logic	A DC voltage is superimposed on U_x

Signal Description	Test Point	Functional Group in the Block Circuit Diagram (Figure 10-19)	1-Signal Signifies
ST	IC 2611/4.1 pin 3	Start/Stop Circuit	Start push button is pressed
$\overline{V}$	IC 2615/4.1 pin 1	Scoring logic	Advance is turned on
U_x	Connection Point 15	U_x amplifier	Swept voltage from sub-assembly (16)
U_x	TP 2607	U_x amplifier	DC voltage superimposed on U_x after the amplifier
U_{ASZ}	Connection Point a	Swept voltage generator	Swept voltage of the recorder assembly at the comparator imput

Table 10-3 Control Signals in the Recording Assembly and Cycle Plan Sub-assembly



Key for Figure 10-24:

Hüllkurve	=	Enveloping Curve
Ablauf	=	Cycle
1. Halbbild	=	First field
Eichen oben	=	Calibration at top
Linkes Bild	=	Left image
Spring	=	Jump
Vorlauf	=	Advance
Rücklauf "Messen"	=	Reverse traverse "Measuring"
Rücklauf schnell	=	Rapid reverse traverse
Eichen	=	Calibrating
Messen	=	Measuring
Schreiben	=	Recording

Fig. 10-24 Cycle Plan of Recording Assembly

10.2.26 BF LEVEL METER (Accessory, only supplied upon request)

10.2.26.1 RF Amplifier, Rectifier and Discriminator (32)

The RF amplifier is a controllable 5-stage amplifier with an input impedance of 75 Ω.

The input signal passes through the 1 kHz high-pass filter C 3201/ R-3202 to the first amplifier stage T 3201 with $v_o \approx 2$, which also contains the 1 dB attenuator stage switched by G1 3201.

The high-pass filter is intended to suppress low-frequency components of the input signal (e.g. deflecting voltage from the the RMS-4), to prevent the first stage from being overdriven so that no modulation occurs with the test signal. The second stage T 3202 with $v_o \approx 2.5$ contains the 20 dB attenuator. Decoupling to the next stage is carried out by means of very highly resistive feedback amplifier T 3203 and T 3204 which also contains the 10 dB attenuator ($v_o \approx 7$). The RC-series connection R 3228/C 3217 limits ring amplification at high frequencies. Amplifier stage T 3205 ($v_o \approx 2$) contains the 2, 4, 6 and 8 dB attenuators These are then followed again by a feedback amplifier T 3206 and T 3207 for decoupling.

With the exception of the 1 dB attenuator, the attenuators are switched by relays.

The absolute value (parallel connection of resistors) and frequency response can be alignment for all attenuators with the exception of the 1 dB and 2 dB attenuators. Inductances L 3201, L 3202 and L 3203 provide overall frequency peaking.

The test signal is routed from the RF amplifier to the discriminator and final amplifier circuits.

The feedback output amplifier with T 3209 and T 3211 ($V \approx 10$) generates the level of approximately 3 V_{pp} which is necessary for the "quasi-r.m.s. value rectifier". Components C 3239 and L 3204 provide frequency response correction in the medium and upper frequency range.

The signal for the discriminator is coupled out by emitter follower T 3208 and routed to comparator IC 3201 which supplies rectangular signals with TTL amplitude at the output. Pulses with a width of approxi-

mately 20 ns and the repetition frequency of the input signal are generated in the subsequent monoflop IC 3202/ 4.1...4.4.

The pulses are rectified by G1 3204/G1 3205. The output voltage ($\hat{=}$ deflecting voltage during sweep operation) is amplified by IC 3205 and conducted via [29] (S 1601/ II) of the $U_{x\text{-generation}}$ circuit (16).

10.2.26.2 DC Voltage Processing Circuit (32)

The rectifier and the DC voltage processing circuit are designed for a usable level range of ±1 dB. This corresponds to a rectifier output voltage of ≈ -950 mV ±100 mV. The output signal from the rectifier passes through an active 1 kHz low-pass filter (IC 3204/4.2) to suppress residual RF components and noise components to the IC 3204/4.3 and is amplified to approximately 4 V. The Level Meter is calibrated by potentiometer [41] (P 3203).

The mean output voltage from the rectifier is shifted to 0 V by IC 3204/4.4 and the usable range thus becomes symmetric about zero. After additional amplification by IC 3204/4.4, the usable range corresponds to an output voltage range of approximately ±5 V at IC 3204/4.4. The output signal from IC 3204 is logarithmized by diode G1 3207. As the usable range is zero symmetric ±1 dB, a diode kink is sufficient for logarithmization at 0 V. The second diode G1 3208 provides temperature compensa-tion of the threshold voltage, so that the kink point remains constant. IC 3206/2.1 serves as a buffer stage for the logarithmizer and facilitates fine correction of amplification. The usable range within the operating range of the digital voltmeter is shifted on the display circuit (34) by IC 3206/2.2 so that ±1 dB corresponds to 0... -2 V. The output signal is routed through a low-pass filter R 32126/C 3264 to the control circuit (33). For representation on the display screen via "Y_{ext}", the ±1 dB range must again correspond to a zero symmetric voltage range; shifting is carried out by R 32124/R 32125. R 32127 and R 32128 act as voltage dividers to the 10 kΩ input impedance of the Y_{ext} amplifier IC 2203 with a sensitivity of 10 mV/display screen.

10.2.26.3 Control circuit (33)

Figure 10-25 shows a basic circuit diagram of the control circuit. RF amplifier, rectifier, DC voltage processing circuit (32) and the control circuit (33) form an automatic control circuit. The voltage at the output of the DC voltage processing circuit is adjusted by the attenuators in the RF amplifier so that it lies within the

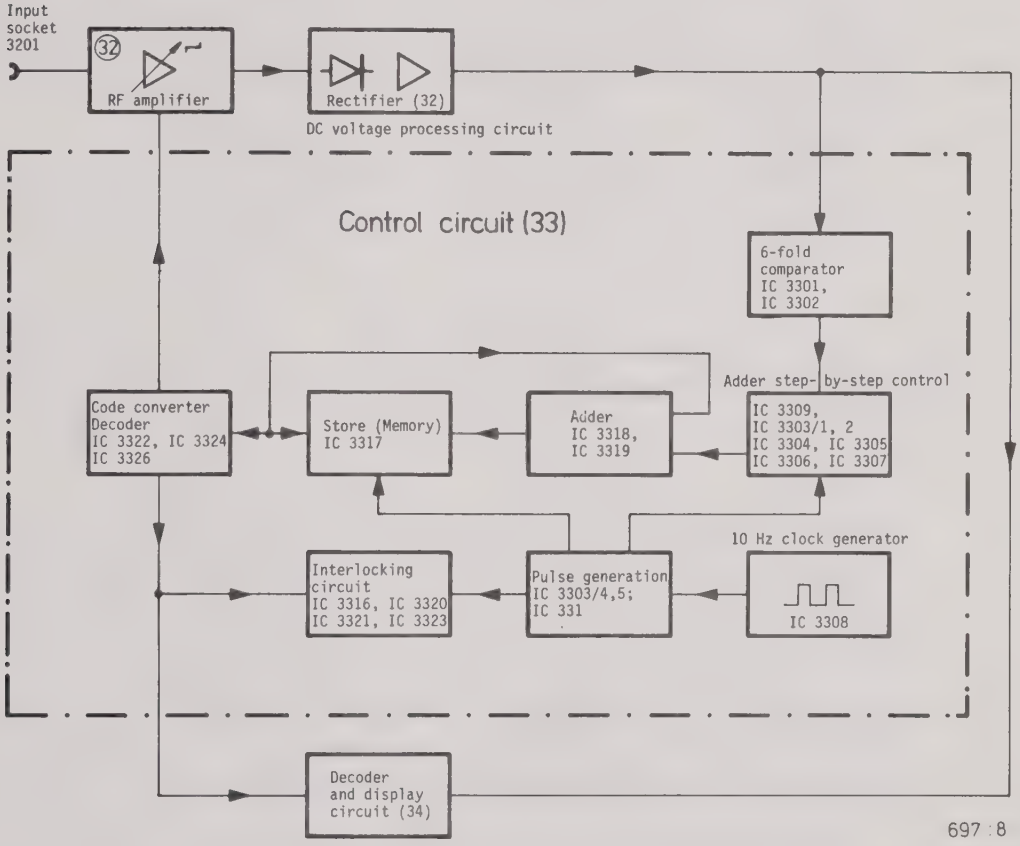

Input socket 3201
32
RF amplifier
Rectifier (32)
DC voltage processing circuit
Control circuit (33)
6-fold comparator IC 3301, IC 3302
Adder step-by-step control IC 3309, IC 3303/1, 2 IC 3304, IC 3305 IC 3306, IC 3307
Adder IC 3318, IC 3319
Store (Memory) IC 3317
Code converter Decoder IC 3322, IC 3324 IC 3326
10 Hz clock generator
IC 3308
Pulse generation IC 3303/4,5; IC 331
Interlocking circuit IC 3316, IC 3320 IC 3321, IC 3323
Decoder and display circuit (34)
697 : 8

Fig 10-25 Control ciruit (33)

range 0...-2 V (providing input level lies within the usable range -10...-51 dBm). The control function is provided by the 10 Hz internal clock from IC 3308/1.1.

The control cycles are divided into two phases: attenuators step-by-step control (control clock) and storage of the current attenuator value (storage clock). Transfers of the attenuator step-by-step control IC 3309 and storage of the attenuator value IC 3317 are carried out in half a clock pulse period shifted by pulses which are approxi-

mately 100 ns wide. This enables the avoidance of noise caused by relay contact bounce, by resonance from the RF amplifier and rectifier and by noise in the voltage from the output of the DC voltage processing circuit.

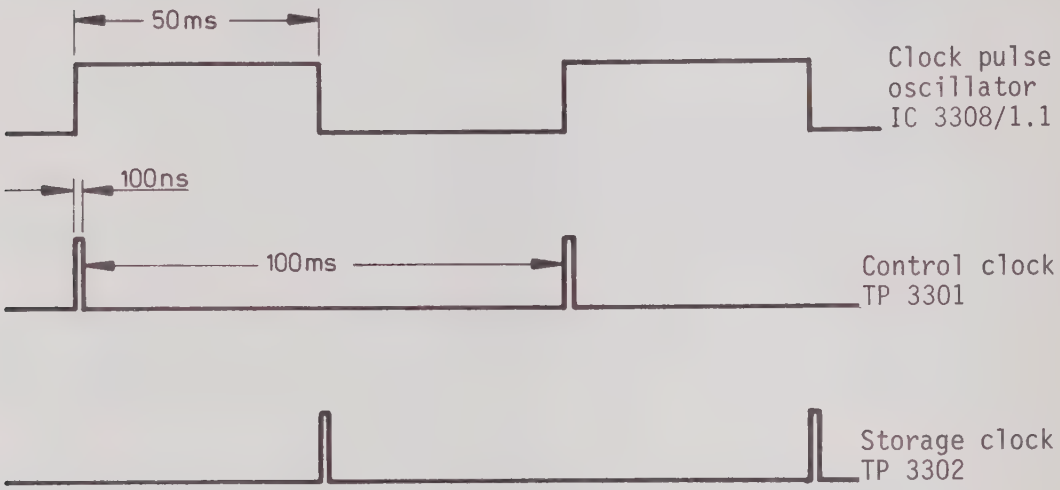


Figure 10-26 697:9

The voltage from the output of the DC voltage processing circuits is evaluated by a 6-fold comparator (IC 3301 and IC 3302). Schmitt triggers are subsequently connected to the comparator outputs to achieve the edge steepness necessary for TTL logic. Figure 10-27 shows the position of the comparator thresholds and explains the control functions derived from them. The function of the 1 dB hysteresis area at the edge of the DVM display range in each case is to prevent continuous starting of the level search routine caused by noisy measuring results or results superimposed with interference and constant to-and-fro switching of the 2 dB attenuator at the range boundary.

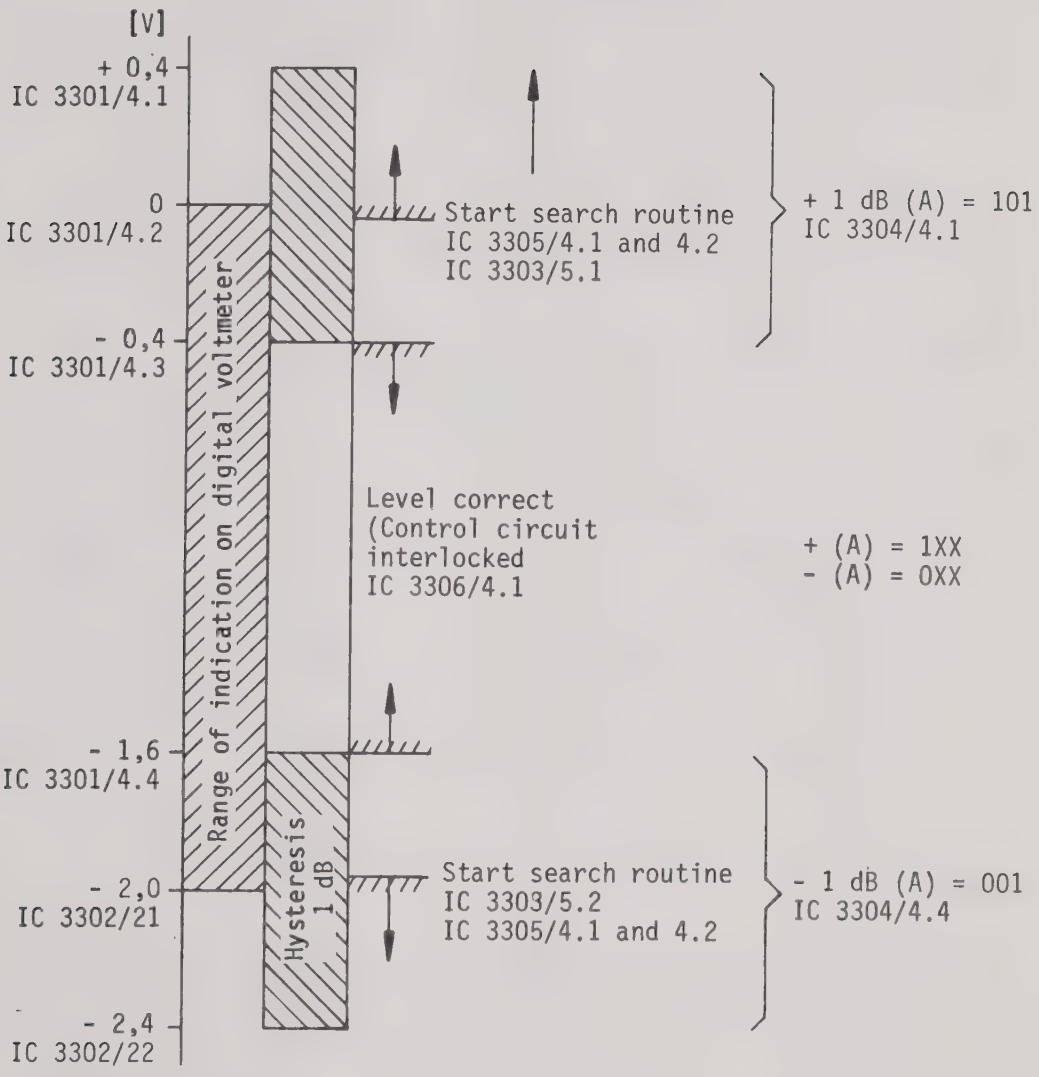


Figure 10-27

The level search routine is hierarchically controlled by the attenuator step-by-step control circuit IC 3309 to keep the number of switching steps as low as possible. Figure 10-28 shows the attenuator control function resulting from input information "level above the range of indication $\uparrow V_{in} > -0.05$ V" and "level below the range of indication $\downarrow V_{in} < -1.95$ V". The values shown are the attenuator values in dB (attenuation).

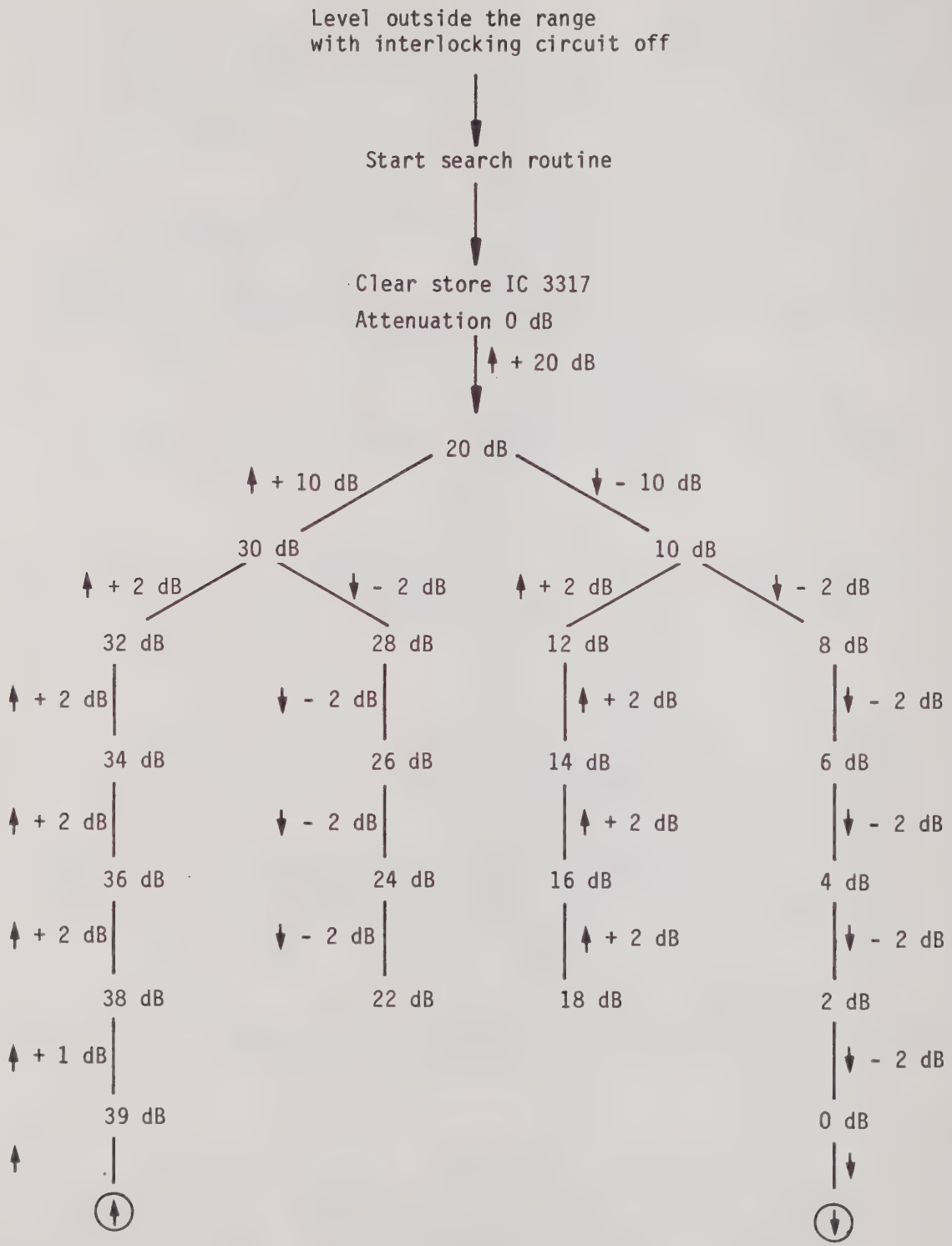

Level outside the range
with interlocking circuit off
Start search routine
Clear store IC 3317
Attenuation 0 dB
+ 20 dB
20 dB
+ 10 dB
- 10 dB
30 dB
10 dB
+ 2 dB
- 2 dB
+ 2 dB
- 2 dB
32 dB
28 dB
12 dB
8 dB
+ 2 dB
- 2 dB
+ 2 dB
- 2 dB
34 dB
26 dB
14 dB
6 dB
+ 2 dB
- 2 dB
+ 2 dB
- 2 dB
36 dB
24 dB
16 dB
4 dB
+ 2 dB
- 2 dB
+ 2 dB
- 2 dB
38 dB
22 dB
18 dB
2 dB
+ 1 dB
- 2 dB
39 dB
0 dB

Figure 10-28

The first FF is set by IC 3309 with the control clock after requesting the information "start search routine" (IC 3303/5.1 = "1" or IC 3303/ 5.2 = "1"⟶IC 3305/ 4.2 = "1"). This clears store IC 3317 via monoflop IC 3310, i.e. the RF amplifier (32) is switched to maximum gain. The duration of the clear pulse is chosen so that a drop-out of the relay used in the RF amplifier is safely bridged (t_{clear} = 1 ms > t_{ab} = 0.7 ms max.). The storage clock for IC 3317 is released by IC 3307 with the second control clock after "start search routine". The attenuator steps are controlled by means of the information from the FF's IC 3309/4.3 and 4.4. The address for the multiplexer IC 3312 ...IC 3315 acting as a read-only memory is obtained from the information from the two FFs and the information at IC 3304/4.3. 5 bit and 1 sign bit are necessary for binary representation of the divider steps (max. decimal value +20, see also graph in Figure 10-28). The sign bit is transferred directly from the Schmitt trigger IC 3304/4.3 via IC 3316/3.1. The 5 value bits are selected by the multiplexer IC 3312... IC 3315. Since bits 3 and 5 are identical for the required binary values, only 4 multiplexer modules are needed. The assignment of the multiplexer is shown in the following Table 10-4.

Negative divider step values are represented by the two's complement.

Address C	B	A	bit 6 (sign) IC 3315/3.1	bit 5 (IC 3313)	bit 4 IC 3312	bit 3 IC 3313	bit 2 IC 3314	bit 1 IC 3315	Value
0	0	0	1	0	0	0	0	0	-0
0	0	1	1	1	1	1	1	1	-1
0	1	0	1	1	1	1	1	0	-2
0	1	1	1	1	0	1	1	0	-10
1	0	0	0	1	0	1	0	0	+20
1	0	1	0	0	0	0	0	1	+1
1	1	0	0	0	0	0	1	0	+2
1	1	1	0	0	1	0	1	0	+10

Table 10-4

With the first store clock, the value selected by the multiplexer (IC 3312...IC 3315) +20 is transferred via the adder IC 3318 and IC 3319 into the store. With the third control clock after "start search routine" (IC 3309/4.3 = 1), +10 or -10 is selected accordingly at the multiplexer (IC 3312...IC 3315), added to the current attenuator value and newly stored. With the fourth control clock after "start search routine" (IC 3309/4.4 = 1 $\hat{=}$ $\overline{Q}$ = 0), +2 or -2 is selected accordingly at the multiplexer, added to the attenuator value and newly stored. The routine continues in steps of 2. The decision whether a positive or a negative attenuator step value is selected, i.e. whether the value is added or subtracted, is made by comparator IC 3301/4.4 (-1.6 V threshold). If the value of the voltage from the output of the DC voltage processing circuit (32) falls within the 1 dB hysteresis area (see Figure 10-27), +1 or -1 is selected accordingly at the multiplier, added to the attenuator value and newly stored. If the output voltage from the DC voltage processing circuit (32) lies within the "level correct" range (IC 3304/4.2 and 4.3), the search routine is terminated by blocking the storage clock for IC 3317 (IC 3306/4.1, IC 3307/3.3). After a further 4 control clocks, the attenuator step-by-step control circuit IC 3309 returns to the starting condition (e, g, i, l = 0, 0, 0, 1). The binary value held in store IC 3317 is recoded into the BCD code by IC 3322 and passes through the relay driver IC 3324 and IC 3326 to the RF amplifier (32). The BCD coded divider value is routed in parallel to the display circuit (34).

Interlocking:

If the level at the input of the RF amplifier lies outside the dynamic range -10...-51 dBm, no level search routine may be run. In this connection, the attenuator value at the output of IC 3322 and the comparator information "input voltage above or, where appropriate, below the range of indication" is evaluated by IC 3320/3.2 and 3.3, IC 3321 and IC 3316/3.2 and 3.3. The following conditions lead to interlocking:

- attenuator value zero (no attenuator activated in the RF amplifier) and input voltage below the range of indication. IC 3320/3.2, IC 3320/3.3

- attenuator value 39 (all attenuators in the RF amplifier activated) and input voltage above the range of indication (> -0.05 V) IC 3321/3.3, IC 3323/4.1
- S 3401 in position " ΔP_{BF}" (sweep operation) IC 3323/4.2...4.4

The interlocking circuit also brings about selection of +1 at the multiplexer IC 3312...IC 3315 if the current attenuator value is 38 dB and the input voltage lies above the range of indication and outside the 1 dB hysteresis area.

If the attenuator value is 39 dB, the clock for store IC 3317 is blocked. This also applies if the input voltage lies outside the "level correct" range (see Figure 10-27). If a change in level occurs at the input before the first FF is set by IC 3309 to "0", the clear-phase for store IC 3317 is omitted; the store remains locked, although the voltage at the input is too low (> -2 V). This interlock is cancelled by IC 3303/5.3, IC 3305/4.3, C 3316 and R 3338. If the storage clock is blocked (all attenuators in the RF amplifier (32) activated) and "level below" information (IC 3303/2) is provided at the input, monoflop IC 3310 receives a short pulse; store IC 3317 is cleared. A new search routine is now started.

10.2.26.4 Display Circuit, Decoder (34)

The digital information concerning the setting of the attenuators in the RF amplifier (32) and the analog value from the DC voltage processing circuit (32) are processed in the display circuit and in the decoder and are displayed by liquid crystal display IC 3413.

Analog Section:

The output voltage from the DC voltage processing circuit (32) is routed to Point 31 of the integrated 3 1/2-digit digital voltmeter IC 3415. IC 3415 has an operating range of $\pm$1.999 V, which is only utilized on one side from 0...-1.99 V and with 2 1/2 display positions (10 mV position $\hat{=}$ 0.01 dB $\hat{=}$ last display position). Since positive voltage values are not permitted, it must be ensured that the display cuts off when 0 V is exceeded in the positive direction, i.e. the input voltage of the DVM must be switched to >2 V. This occurs with the aid of comparator IC 3414 and diode G1 3402. If 0 V is exceeded, the

comparator switches to +5 V at the output, G1 3402 becomes forward-biased and therefore approximately +4 V are present at the DVM input (Point 31). If the input voltage is negative, G1 3402 is blocked. The LEDs "level too high" G1 3406 and "level too low" G1 3407 are switched via the overflow facility of the digital voltmeter (automatic cut-off of the display if the range is exceeded). The following criteria apply:

Level too high ≙ voltage at DVM > 0 V ≙ -sign cut off
Point 20 IC 3415

Level too low ≙ voltage at DVM < -2 V ≙ no display and no sign "No display" signifies the fact that the segments b and c (Point 16 and Point 24 IC 3415) are not connected to the 7-segment display.

Evaluation of these switch conditions is complicated as the signals for the display are 50 Hz rectangular clock pulses, the information lying within the phase related to the backplane clock (Point 21 IC 3415).

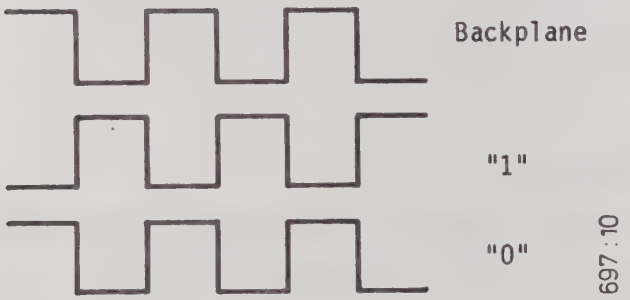


Figure 10-29

The switching signals are compared with the backplane clock for evaluation (NOR operations IC 3418). In the event of logic "1", the inverted clock signal is produced at output "0" and, in the event of "0", the inverted clock signal is present at the output. Static "1" is produced after peak value rectification (G1 3403... G1 3405).

The display cut-off information for the first two display positions which are not triggered by the digital voltmeter are obtained by IC 3419/2.2 from the switch signals for the LEDs G1 3406 and G1 3407. The overflow facility for the first two display positions is triggered by the AND gates IC 3409 and IC 3410 and the 7-segment decoders IC 3411

and IC 3412. If the overflow facility is triggered, "1" is present at all outputs of IC 3409 and IC 3410. This input combination (1 1 1 1) leads in the case of display decoders IC 3411 and IC 3412 to "blank" display.

In sweep operation (switch signal at Point 15 697-CL, sweep operation = "0"), LED's G1 3406 and G1 3407 are switched via comparators IC 3416/2.1 and IC 3416/2.2 and the Schmitt triggers IC 3417/3.1 and IC 3417/3.3. The comparators lie at the range limits 0 and -2 V. In sweep operation, the digital voltmeter indicates the mean value of the input voltage and thus detects no short-term exceeding of the range.

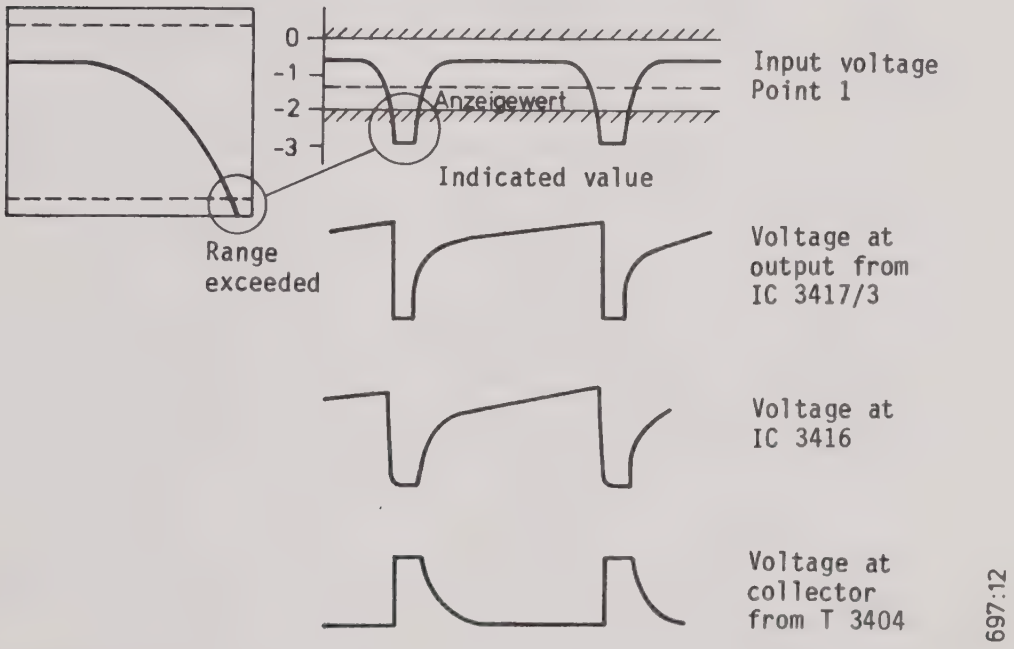


Figure 10-30

Digital Section:

The attenuator information from the control circuit (33) is converted in the digital section to absolute level values. The 1 dB position is converted by IC 3402/ 5.1...5.3, IC 3403/3.1, IC 3404/3.1.

The 1 dB carryover of the digital voltmeter pin 19 IC 3415 is counted into the displayed value in adder IC 3405. IC 3409 controls the 7-segment decoder IC 3412 for the 1 dB position on the LCD display. IC 3407/4.1 and 4.2 and IC 3406/3.1 process the amount carried over into

the 10 dB position. Recoding and processing of the carryover for the 10 dB position is performed by IC 3402/5.4 and 5.5, IC 3403/3.2, IC 3406/3.2 and 3.3, IC 3404/3.2 and 3.3.

IC 3410 controls the 7-segment decoder IC 3411 for the 10 dB position on the LCD display.

10.2.26.5 Calibrated oscillator (34)

The calibrated oscillator is a Meissner oscillator whose amplitude of oscillation is stabilized by the reference diode G1 3401. The frequency is 100 kHz. The output signal is coupled out by O 3401 with $\approx$ Z_{out} = 0, attenuated to -30.00 dBm by attenuators P 3401/R 3412/R 3413/ R 3414 and matched to Z = 75 Ω. (-30.00 dBm applies for termination with Z = 75 Ω).

10.2.27 Display Unit ST-1

10.2.27.1 Retrace Blanking (2)

The Wehnelt cylinder of picture tube RÖ 401, connection 3, can be switched over the transistor T 201 to a potential, which is sufficiently negative relative to the cathode that electrons can no longer emerge, that is, the CRT screen remains dark. This effect insures that the electron beam is not visible during the reverse traverse.

In order to avoid punctiform poisoning of the luminous layer when X and Y swept signals are absent, the electron beam is also suppressed in the absence of an X swept signal.

The potential separation between high and low voltages is accomplished over the optical coupler IC 204.

The X swept signal, coming from the X-Y amplifier (3) is divided in the ratio of 10:1 by the resistances R 201 and R 204 at the input of the comparator IC 201. The switching threshold of the comparator lies at +50 mV; it is determined by R 206 and R 207. The hysteresis, determined by R 210 and R 207, is about 30 mV. The diodes Gl 201 and Gl 202 limit the input voltage of the comparator in case the X input is overloaded.

If the X swept signal is sufficiently large ($>1\ V_{pp}$), the switching threshold of the comparator is exceeded and impulses appear at its output, with which the monoflop IC 202 is triggered. IC 202 is a retriggerable monoflop, whose relaxation time (about 1 s) is greater than the duration of the cycle of the smallest possible swept frequency of 18 Hz. The output (pin 8) of IC 202 therefore constantly carries a HIGH signal when an X deflection is present.

This HIGH signal opens the gate IC 203/4.1 for the blanking pulses at its input (pin 2). If there is no LOW signal at pin 5 of IC 203/4.2, the blanking pulses appear in inverted form at the output of IC 203/4.3, pin 11. During a LOW signal at pin 3 of the optical coupler IC 204, the phototransistor at the output of the optical coupler is conductive, as a result of which the transistor T 201 is blocked. In case transistor T 201 is blocked, the position of the wiper of potentiometer [3] (P 206) determines over the Darlington emitter follower T 202, T 203 the potential,

at its collector, that is, the potential of the WEHNELT cylinder of the picture tube Rö 401, connection 3. Initial and final values of the range, which can be adjusted with potentiometer 3 (P 206), can be set with the help of potentiometers P 204 and P 205.

During a HIGH signal at the output of the optical coupler IC 204, pin 3, the output transistor is blocked, that is, T 201 is conductive. In the interest of short switching times, the diode Gl 205 ensures that the collector emitter voltage is about 2 to 3 V and does not decrease to the saturation voltage. The voltage of the WEHNELT cylinder, which is connected to the collector of T 201, is therefore close to -1.35 kV, that is, it is about 100 V more negative than the voltage of -1.25 V at the cathode. This voltage is sufficient for preventing electrons reaching the anode, that is, the CRT screen remains dark. The diode Gl 206, poled in the blocking direction when transistor T 201 is conductive, prevents destruction of the base emitter spaces of T 202 and T 203.

The bridging of the resistances R 220 and R 221 by the capacitor C 205 provides for a rapid connection of T 201 in the circuit.

Should there be a short circuit between the WEHNELT cylinder and the grounded first acceleration electrode of the picture tube, diode Gl 207, which is poled in the forward direction, prevents a voltage arc-over between the WEHNELT cylinder and the cathode.

The part of the circuit "bright intensification option" has no bearing on the operation of the display unit in the RME-4.

10.2.27.2 X-Y Amplifiers (3)

The amplifiers produce the X or Y deflection voltages for the electrostatic deflection of the beam from the X or Y input signal. Except for the resistive divider before the final stages, the circuits of the amplifiers are the same. For this reason, only the X amplifier is described in the following.

The input amplifier IC 305 functions as a buffer stage and impedance converter. Because of the greater output bandwidth, the amplifier is operated with V = 10. The input divider R 368, P 306, R 367 divides the nominal input voltage of $\pm$ 2.5 V_p for full modulation downwards to such an extent, that the voltage at the output of IC 305 is $\pm$ 2 V_p. The amplification tolerances of the total X amplifier and the tolerance of the deflection coefficient are balanced with P 306, which controls image width. The impedance converter IC 306 takes the X shift voltage (X zero line) at a low resistance from potentiometer [5] (P 308) to the input stage IC 305 (no change in amplification from IC 305 through (P 308)).

The linearization stage IC 302, with V = 2, follows the input stage. Because of the limited output bandwidth of IC 302, the signal is divided by the divider R 334, R 338, R 358 in the ratio of 4:1.

In the linearization stage, the amplification is increased or decreased depending on the polarity and modulation and inversely according to the linearity distortions of the picture tubes. The

characteristic line of the amplifier can be distorted with 2 different slopes separately for the positive and the negative amplitudes. The amplification is decreased by connecting the resistances R 322, R 326, R 329, R 332 in parallel to R 333, while it is increased by connecting R 340, R 342, R 346, R 350 in parallel to R 337. By soldering diodes and bridges to the corresponding points aa to dc or a to f, the desired distortion is set. The onset point of the distortion is set by potentiometers P 302, P 304, P 305, P 307. For the purpose of decoupling, each potentiometer is followed by an amplifier (IC 304/3.1 to 3.4), at which the temperature compensation for the linearization network is carried out with the help of the diodes Gl 305 and Gl 306 (bridges a to f). Gl 301 and Gl 302 stabilize the linearization against variations in the supply voltage.

The limiting circuit T 303 and T 304 intervenes between the input stage and the linearization stage. The limiting circuit protects the final stage, which can be overloaded only very slightly, from inversion of the signal.

The limitation is accomplished by two complementary base stages. The limitation onset is set by the potentiometers P 301 (negative amplitude) and P 303 (positive amplitude). The limiting circuit is temperature compensated by the diodes Gl 303 or Gl 304.

The output amplifier IC 301/2.1 and 2.2, T 301, T 302 follows the linearization stage. The output amplifier consists of two amplifier branches. Each branch consists of an operational amplifier, followed by an emitter stage to which both are

coupled in opposite directions. The input voltage is supplied to one amplifier branch at the inverting input and to the other branch at the non-inverting input, as a result of which voltages of opposite phases appear at the outputs. The output transistors form a bridge with the collector resistances. The deflecting plates are connected in the collector-collector bridge diagonal. The amplification of each branch is 100, in order to attain a greater output bandwidth. The operating point of the output transistors and therefore of the average plate potential (connection point 3 and connection point 4) are adjusted to about 145 V with the dividers R 315, R 316 or R 313, R 314.

In the case of the Y amplifier, the dimensions of the input divider are different because of the lesser output voltage. The quiescent currents of the collector are stabilized by the stabilized power supply T 309 against fluctuations in the 340 V voltage.

In the case of the X amplifier, the input signal for the monitoring of the beam current (retrace blanking) is branched over the buffer stage IC 303.

10.2.27.3 High-Voltage Part (4)

Converter

A converter in sinusoidal operation is used for producing the high voltages of -1.25 kV or -1.35 kV. It consists of a control oscillator, preamplifier and output stage in a bridge circuit. The voltage of -1.25 kV is controlled to $\pm$0.5%. The post-acceleration voltage of + 3.5kV is obtained by means of a voltage

doubler from the AC voltage for -1.25 kV.

The frequency of the driving oscillator (Meissner oscillator) is determined by C 412, C 413 and the inductance of the primary coil of L 401. It corresponds to the resonance frequency of Ü 401 with attached rectifier circuit. The fine adjustment is made using the adjusting screw of L 401. The emitter resistance R 417 and the diode Gl 403 stabilize the operating point of the transistor T 401 against temperature fluctuations.

The oscillation of the oscillator is coupled out over the secondary coil and supplied to the controllable divider R 422, T 402. In order to keep the distortion factor small, the voltage decrease over T 402 is only about 80 mV. The capacitor C 415 decouples the amplifier IC 403 from the control voltage of the FET transistor T 402. IC 403 functions as a pre-amplifier (V = 10) for the output stage.

In order to attain the doubled voltage swing at transformer U 401, the output stage is designed as a bridge circuit, that is, it consists of an inverting (IC 404/2.1) and a non-inverting branch (IC 404/2.2). Each branch has an amplification of V = 10. The two primary connections of the transformer Ü 401 receive signals of equal magnitude, displaced however by 180°, so that the differential voltage over the primary coil has twice the amplitude. A complementary Darlington push-pull output stage, which works in B operation, is included in the feed back in the inverting as well as in the non-inverting branch of the output stage. Because of the slight load-carrying capability of the outputs of the

operational amplifier, the base resistances of the transistors T 407, T 408, or T 409, T 410 are each replaced by a stabilized voltage supply (T 403, R 436, R 437, R 446; T 404, R 439, R 440, R 447 or T 405, R 441, R 442, R 448, T 406, R 444, R 445, R 448). By so doing, the output of the operational amplifier is subjected only to the load resulting from connecting the internal resistance of the power supply in parallel with the input resistance of the Darlington circuit. In addition, the power supply delivers, independently of the modulation, a constant current until the collector-emitter saturation voltage of the transistor is reached. Because the forward voltage of the diodes Gl 404 and Gl 405 or Gl 406 and Gl 407 is less than the sum of the base-emitter voltages of T 407 and T 411, T 408 and T 412 or of T 409 and T 413, T 410 and T 414, no quiescent current flows through the output transistors (B operation).

The slight transfer distortions of the output signal, which result from this, are taken into account, because the thermal stability of the output stage is at the same time ensured by the B operation. As a result of using operational amplifiers, A DC voltage of only a few mV is delivered at the output of the output stage branches, so that setting the zero position and capacitor-coupling the transformer Ü 401 are not necessary.

The capacitors C 419 and C 420 prevent amplification of the offset voltage of IC 403.

C 418 prevents amplification of the offset voltage of IC 404/2.2. The resistances R 456 and R 457 moderate the reaction of the

rectifying process on the outputs of the final stage.

Rectifier

The secondary side of the transformer Ü 401 has two coils. One of these is used for producing the cathode voltage of -1.25 kV, with the other, the cathode voltage for the brightness control is increased by 100 V to -1.35 kV. Both DC voltages are obtained over a half-wave rectifier (Gl 410, C 427 or Gl 409, C 426). In additional, the 1.25 kV coil supplies the voltage doubler C 425, Gl 408, Gl 411, C 428 for producing the post-acceleration voltage of +2.5kV.

The voltage drop at R 458, caused by the beam current, compensates the change in the post-acceleration voltage when the image brightness is changed. The resistances R 459 and R 460 discharge the capacitors C 426 and C 428 after the instrument is switched off. C 427 is discharged over R 406. Discharging is completed after about 3 s.

A DC voltage of about +7 V, which is increased to -1.35 kV and used for supplying the electronics of the retrace blanking (2), is obtained from the 6.3 V AC voltage of the picture-tube heater over the half-wave rectifier Gl 416, C 429.

Control

A portion of the cathode voltage of -1.25 kV is taken over divider R 406, R 408, P 401 to the inverting input of the regulator IC 401. IC 402 amplifies the (negative) output voltage of the regulator.

The (also negative) output voltage of IC 402 functions as a regulating voltage for the FET transistor T 402, which is operated as a controllable resistance and which, together with R 422, forms a controllable divider for the input voltage of IC 403. The diode Gl 402 protects T 402 from positive gate source voltages.

The output voltage of the regulator IC 401 adjusts itself in such a manner that the differential voltage between inverting and non-inverting input becomes zero, that is, the regulating voltage of T 402 and therefore the output voltage of the final stage is changed until the cathode voltage is such that the voltage, applied over the divider R 406, R 408, P 401 to the inverting input of IC 401 is the same as that applied to the non-inverting input.

The reference voltage at the non-inverting input is supplied by the temperature-compensated Zener diode Gl 401. If the dividing ratio is changed with P 401, the cathode voltage is also changed.

Because of the high amplification, a greater voltage deviation may occur at the output of IC 402 and limit the control range. The offset voltage is therefore balanced with P 402.

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